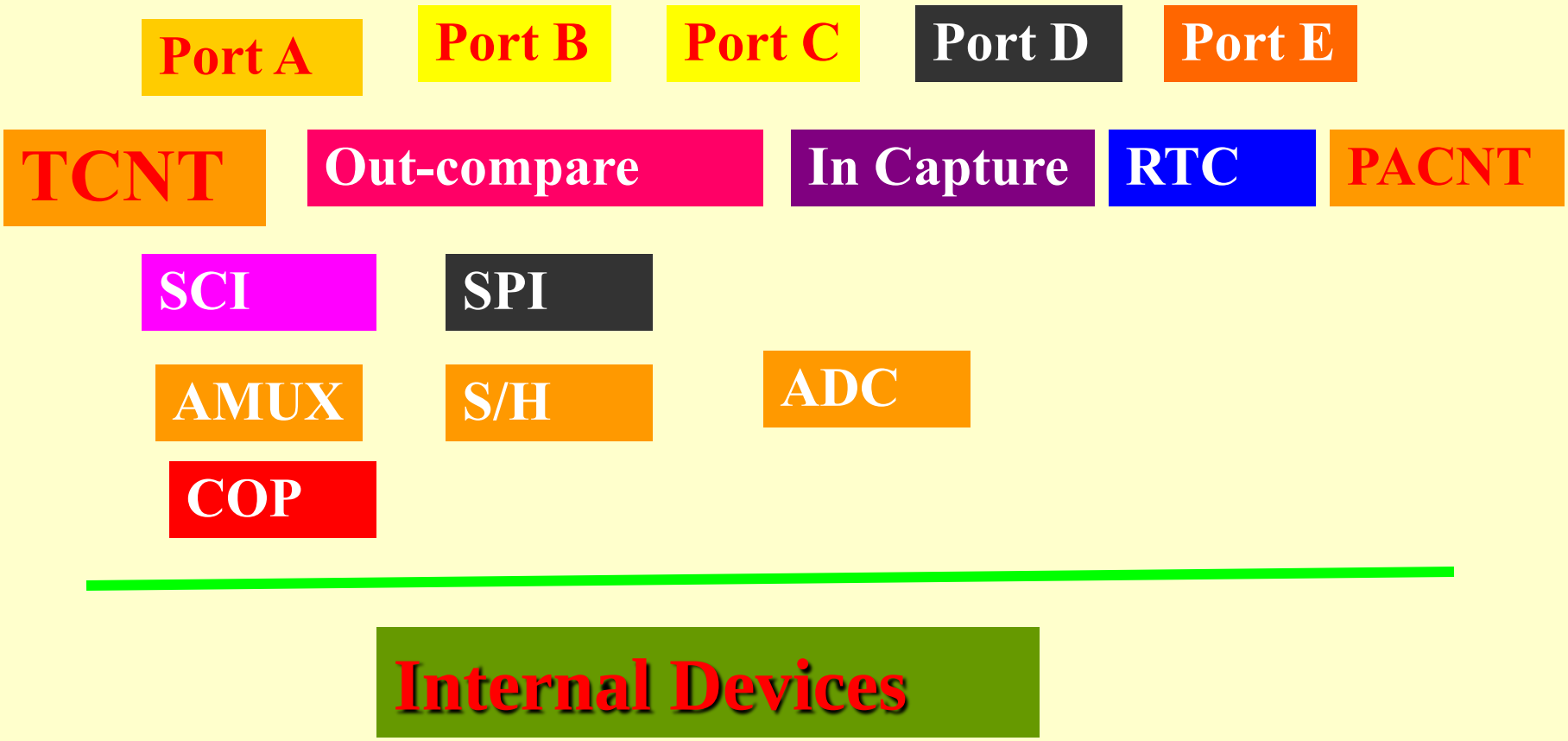
Chapter 16

Motorola MC68HC11 Family MCU Architecture

Lesson 11

PACNT, SPI, SCI, ADC Devices and Interrupt System


Port A
Port B
Port C
Port D
Port E
TCNT
Out-compare
In Capture
RTC
PACNT
SCI
SPI
AMUX
S/H
ADC
COP
Internal Devices

Non Maskable Interrupts

Non Maskable Interrupts: Illegal opcode, CME (clock failure), watch dog timer (NOCOP) interrupt, XIRQ pin XIRQ masks till enable within 64 cycles on reset – highest priorities

Maskable Interrupts

Maskable Interrupts: Port, Real Time Clock, Timer, PACNT, ADC Device Interrupts by enable bits at device register

Interrupt Masks

Primary Mask

By setting I bit or X bit (for XIRQ) in CCR

Secondary Masks

RTI.OC1I-OC5I, IC1I-IC3I, TOI, SPI, RI,TI,ILI, RI, TCI,TEI, ...

Software Interrupts

Software Interrupt:SWI instruction-
Lowest Priority

Interrupt ISR Start and Return

Priority → **Default Assignments**

Push CPU Registers → **PCL, PCH, IYL,IYH, IXL, IXH, ACCA, ACCB, CCR onto stack**

Pre emption → **No in between preemption except by XIRQ if set so**

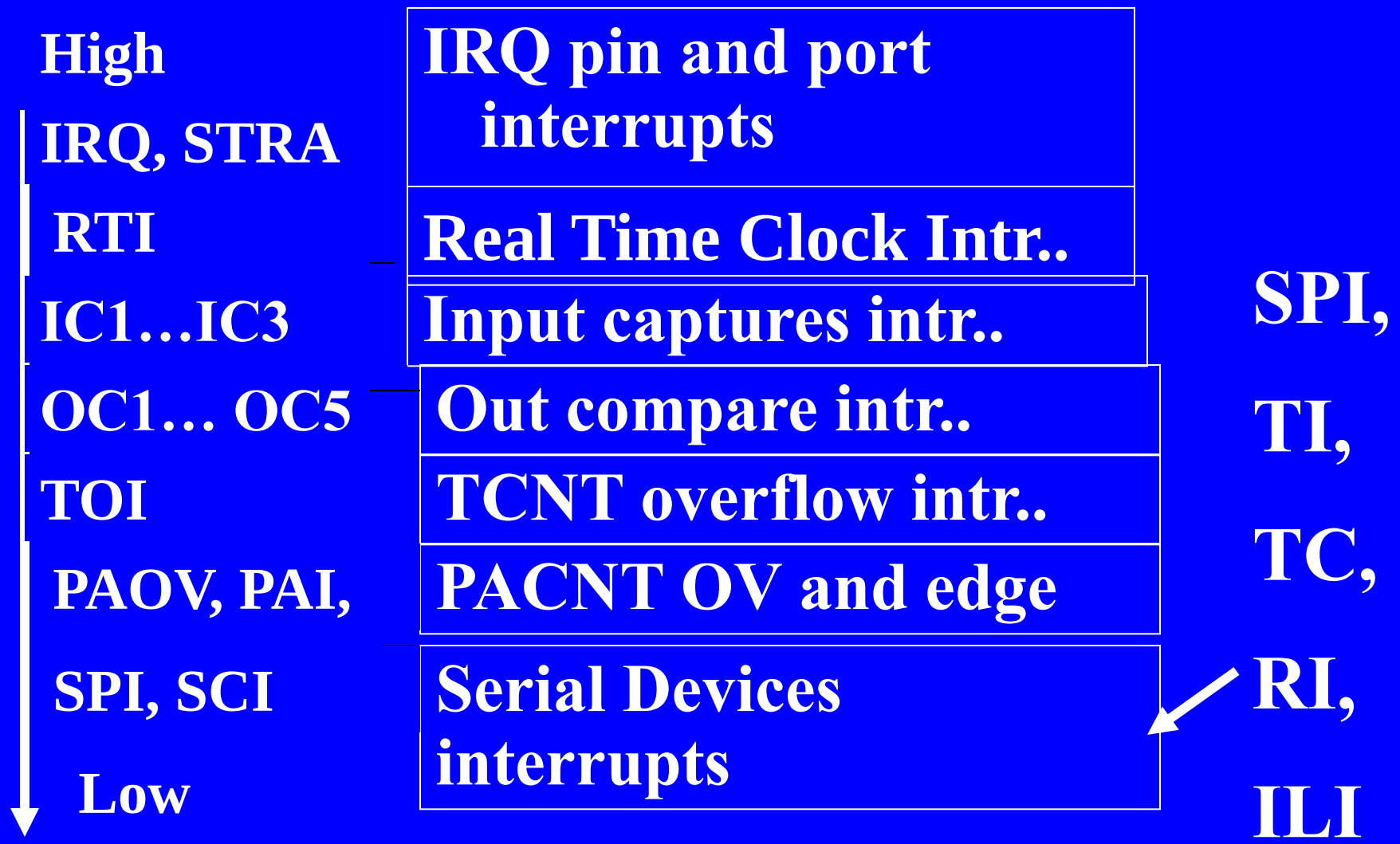
Interrupt ISR Return

Pop CPU Registers → **CCR, ACCB, ACCA, IXH,IXL,IYH,IYL,PCH,PCH from stack**

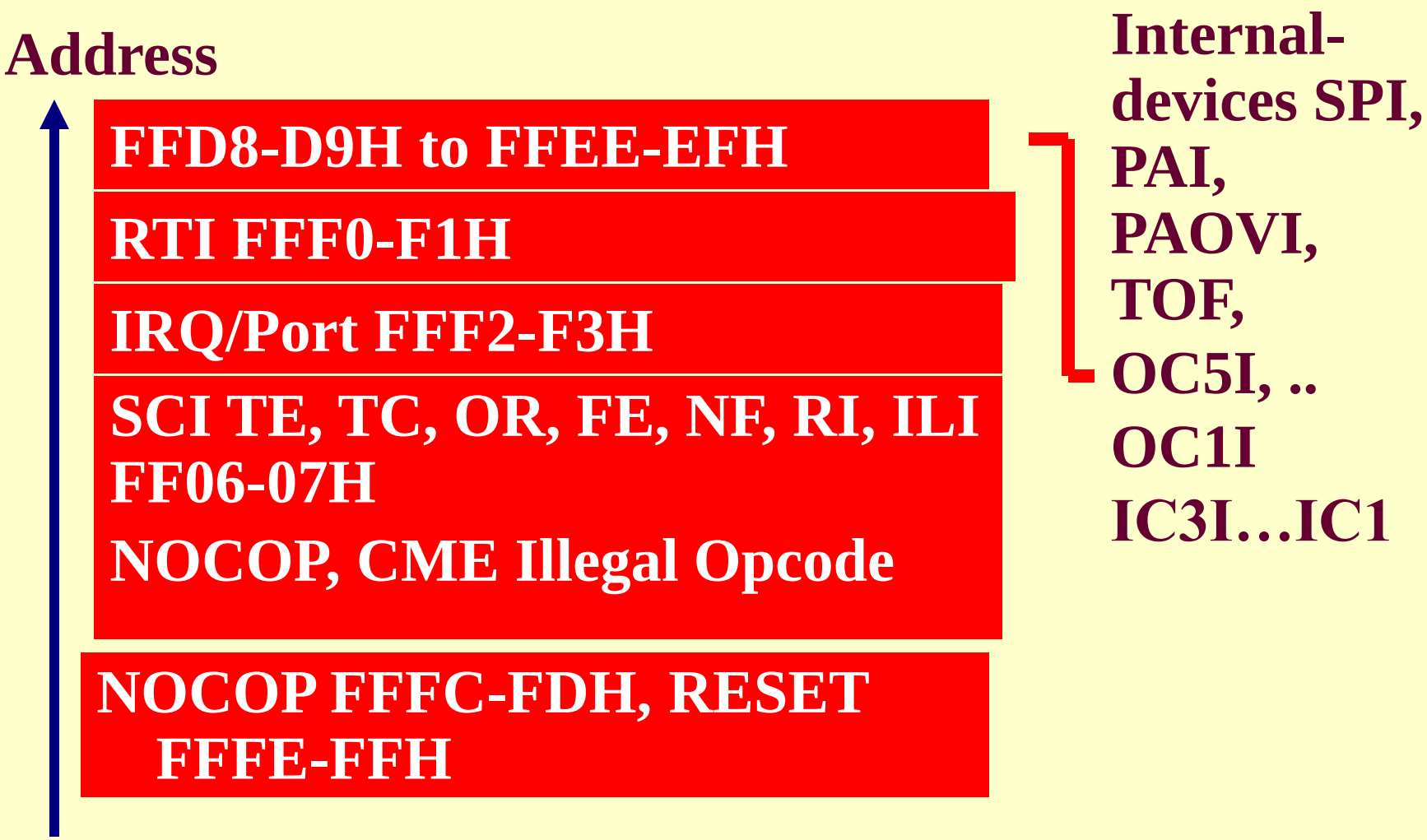
Interrupt Identification

Flags → **For Maskable interrupts**

Maskable Interrupts Priority



Interrupt Vectors



Summary

We learnt

- Register bits
- Interrupts Masks
- Flags
- Interrupt Vectors

End of Lesson 11 on 68HC11 MCU Interrupt System