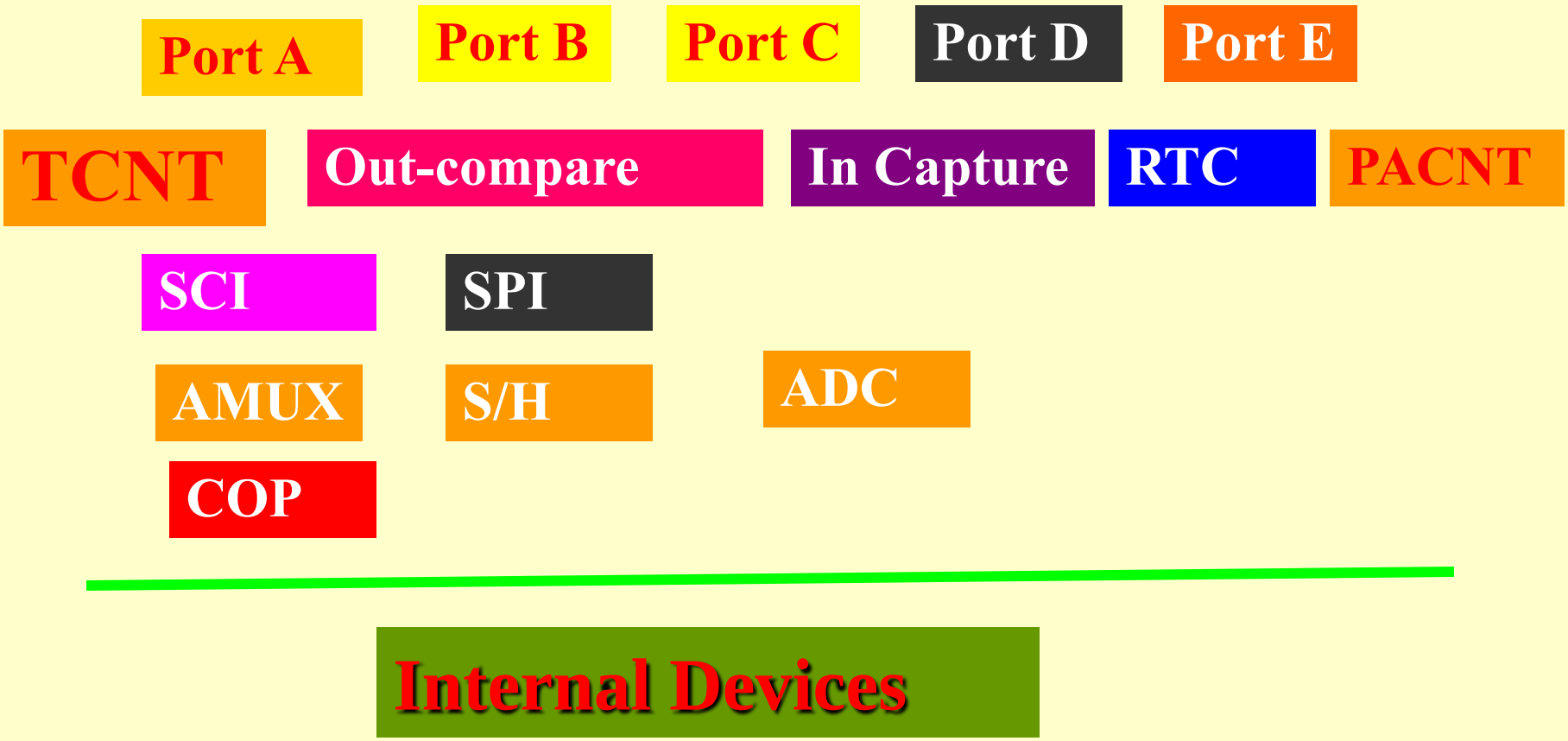
Chapter 16

Motorola MC68HC11 Family MCU Architecture

Lesson 5

System Timing Devices – TCNT, ICs and OCs


Port A
Port B
Port C
Port D
Port E
TCNT
Out-compare
In Capture
RTC
PACNT
SCI
SPI
AMUX
S/H
ADC
COP
Internal Devices

Free running counter TCNT inputs, TCNT overflows and overflow interrupts

16-bit TCNT (Time-Counter)

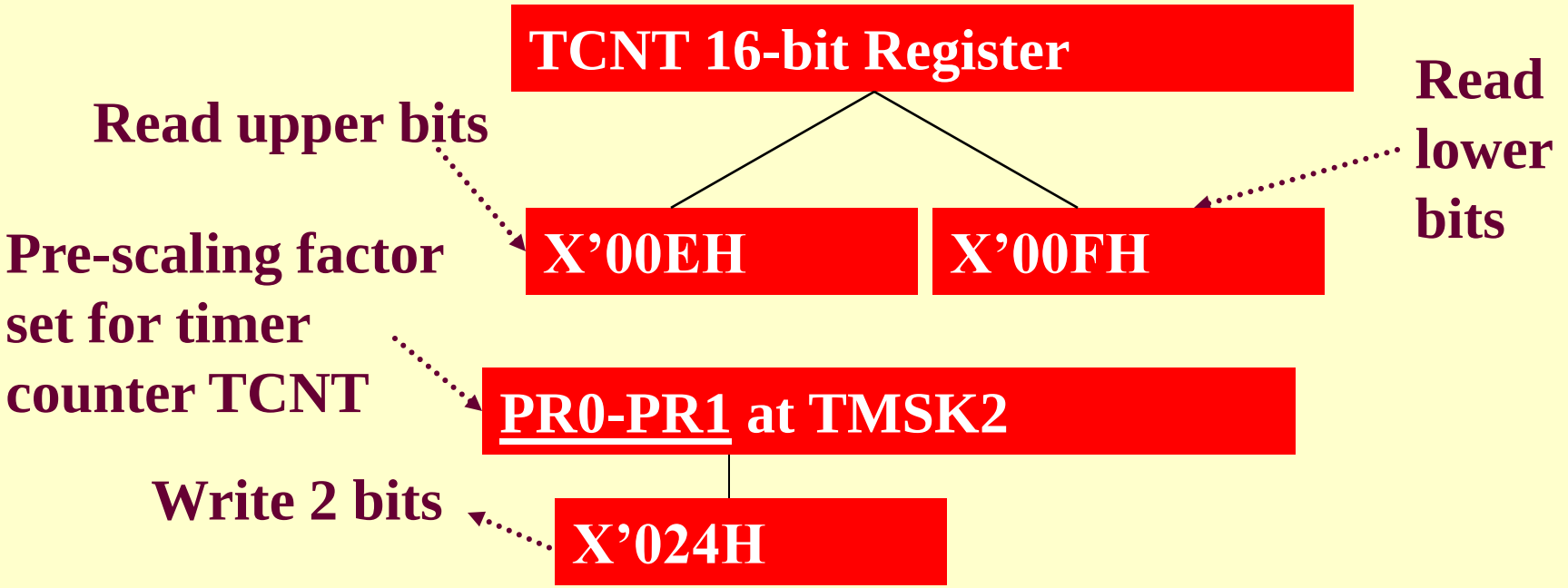
- Free running counter TCNT ← **16- bits**

  gets inputs from E clock (2 MHz for 8MHz XTAL)
- TCNT gets inputs for counting after pre-scaling
- Prescaling means dividing the internal E clock inputs before giving to TCNT
- Period between inputs sets as per PR0-PR1 bits

Prescaling Factor to control TCNT Counts increment and overflow rates

- PR-PR1- predefined within 64 clock cycles after reset
- PR0-PR1 sets pre scaling factor p = 1, 4, 8, 16.
- Period of TCNT inputs = p × 0.5 μs for 8MHz XTAL

Timer-Count Register TCNT and PR0-PR1 bits



X' four bits are as per init register

Interrupt Mask *TCNT OV* Interrupts and Pre-scaling factor set bits TMSK2

PR0-PR1 two bits at TMSK2 at X'024H

Pre-scaling factor set for timer counter TCNT by PR0-PR1

TOI at TMSK2 at x'024H

X' four bits are as per init register

Non Stop Non-resettable

Free running counter

16- bits

TCNT

Successive input periods = p × 0.5 μs for 8MHz XTAL

Successive Overflow periods = 2^{16} × p × 0.5 μs for 8MHz XTAL

Enable TCNT Overflow interrupt

TOI bit at TMSK1

X'024H

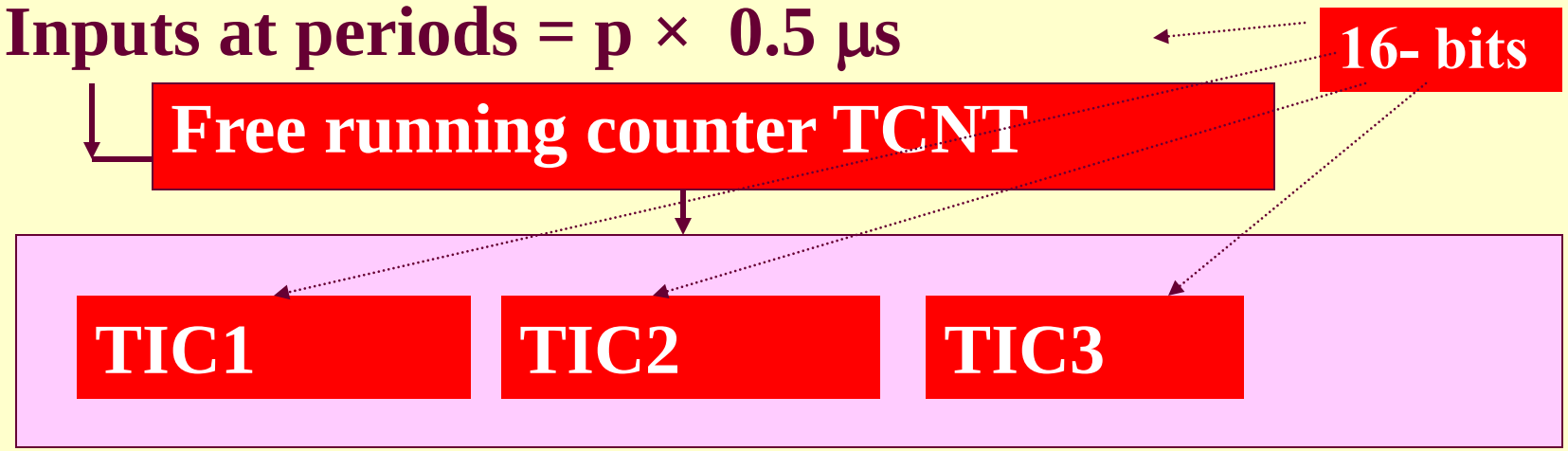
Overflow Flag

TOF at TFLG2

X'025H

Input Captures

Inputs at the Input Capture pins, IC flags and IC Interrupts

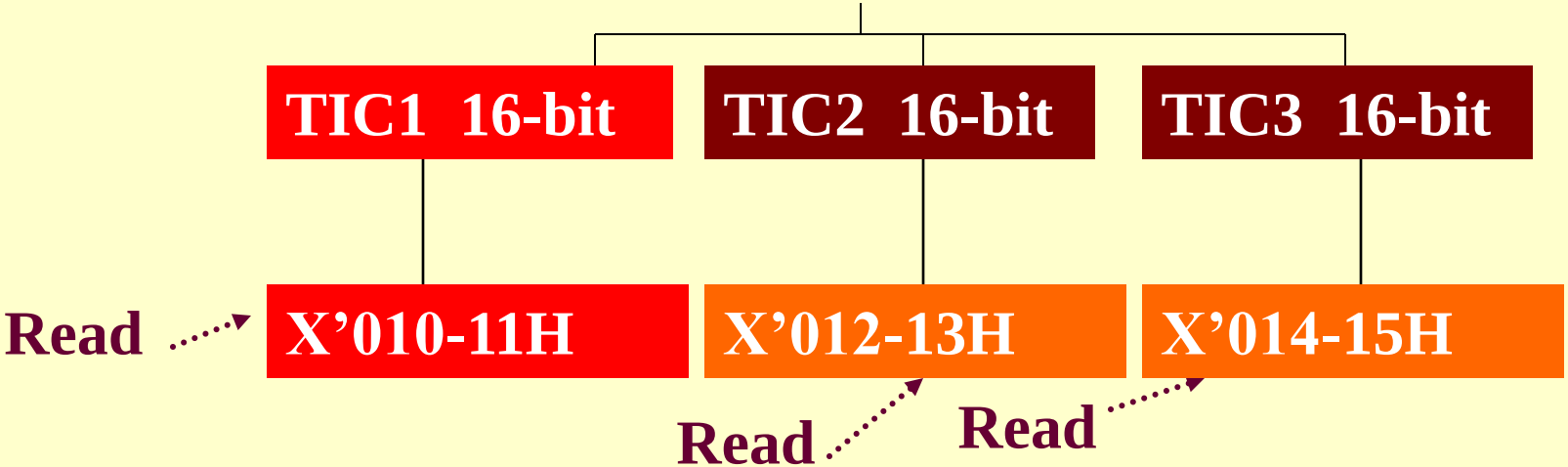


TCNT count values x1, x2 and x3 capture on each inputs at the Pins IC1, IC2 and IC3. The IC1, IC2 and IC3 interrupts occur when interrupts are enabled

Each Capture sets a flag, IC1F orIC2F or IC2F

Each Capture causes interrupt if the capture is not masked using IC1I or IC2I or IC2I

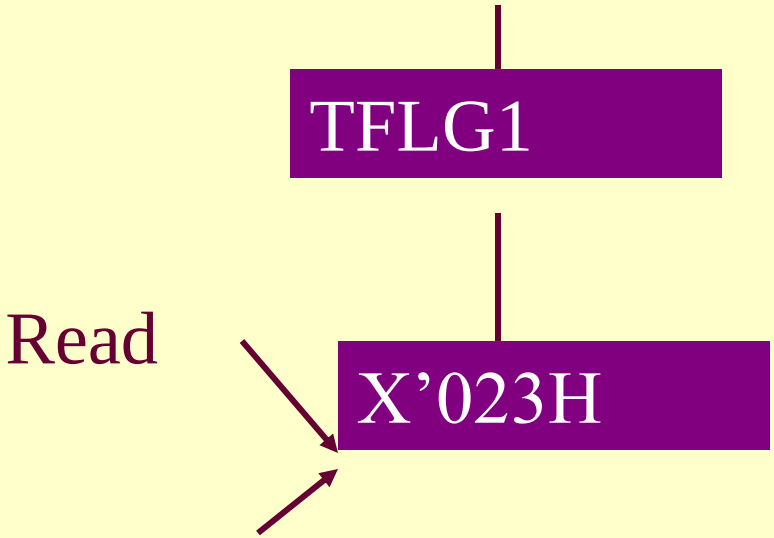
Registers for Time value capture on Input-Capture (s) at IC1 to IC3 pins



A timer Reading captures counts = x at TCNT on an IC pin (s) Interrupt

X' four bits are as per init register

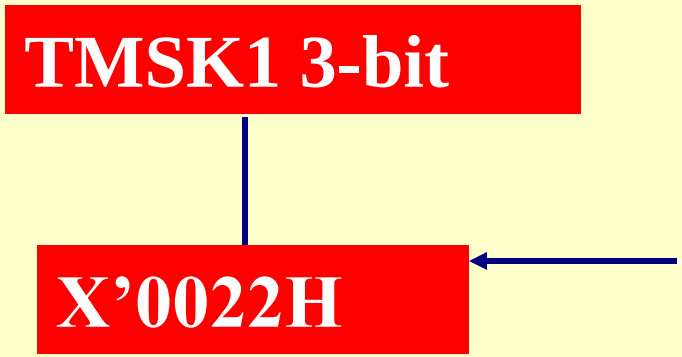
Timer Capture Flags Setting on IC Action Occurrences



IC3F, IC2F, IC1F, bits at TFLG1 at 0023H

X' four bits are as per init register

IC3I, IC2I, IC1I bits at TMSK1 at 0022H



Write for masking or unmasking IC3, IC2 and IC1 interrupts

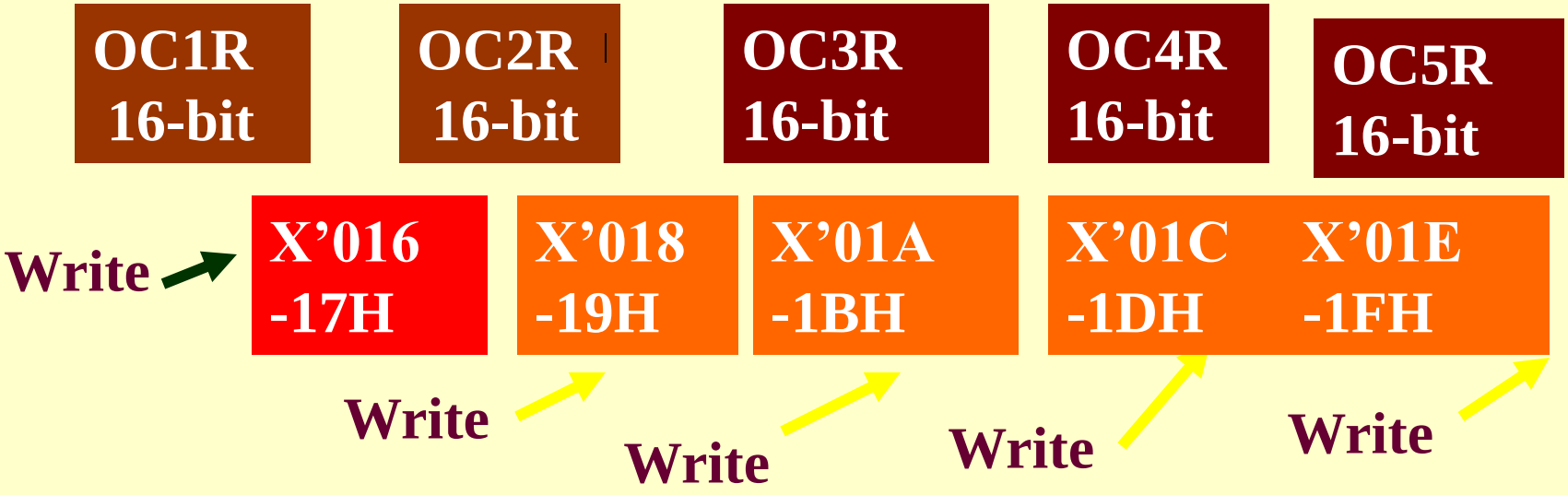
Edg3A, Edg3B, Edg2A, Edg2B, Edg1A and Edg1B bits at TCTL2 at 0021H

An edge +ve or-ve or both +ve and -ve is defined for timer reading and capture action (s) on selected pin(s) between IC1 to IC3 by a write operation at x'021H

Outputs at the Out compare pins, setting of OC flags and the OC Interrupts

OC1 to OC5 actions on OC1 to OC5 Pins, Setting of OC flags and OC interrupts

Registers for Time for an Out-Compare (s) output at pin between OC1 to OC5 pins

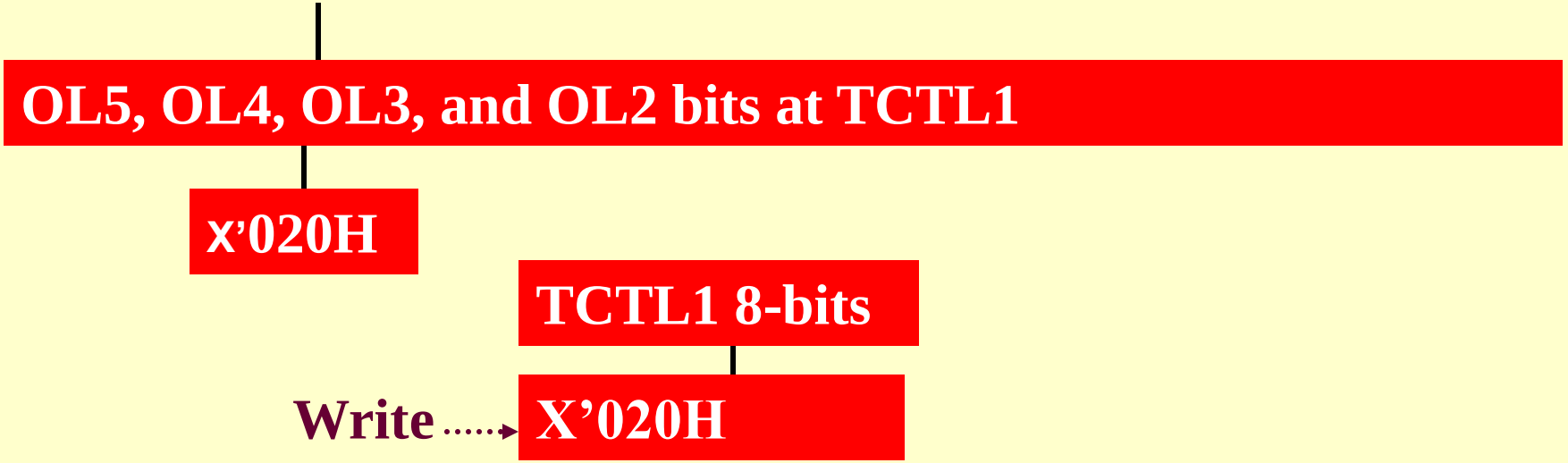


An output OC pin (s) action, OC overflow action(s) and (or) OC interrupt (s) when timer 16-bit reading compares equal with the 16-bit out-compare register(s)

X' four bits are as per init register

Define OCx 2, 3, 4, or 5 output level for OC2 to OC5 Pins

By a write OL operation, the levels (0 or1) for output pin actions are defined for timer reading out compare output action (s) on selected pin(s) between OC2 to IC5



Define OCx 2, 3, 4, or 5 output action-mask bits for OC2 to OC5 interrupts

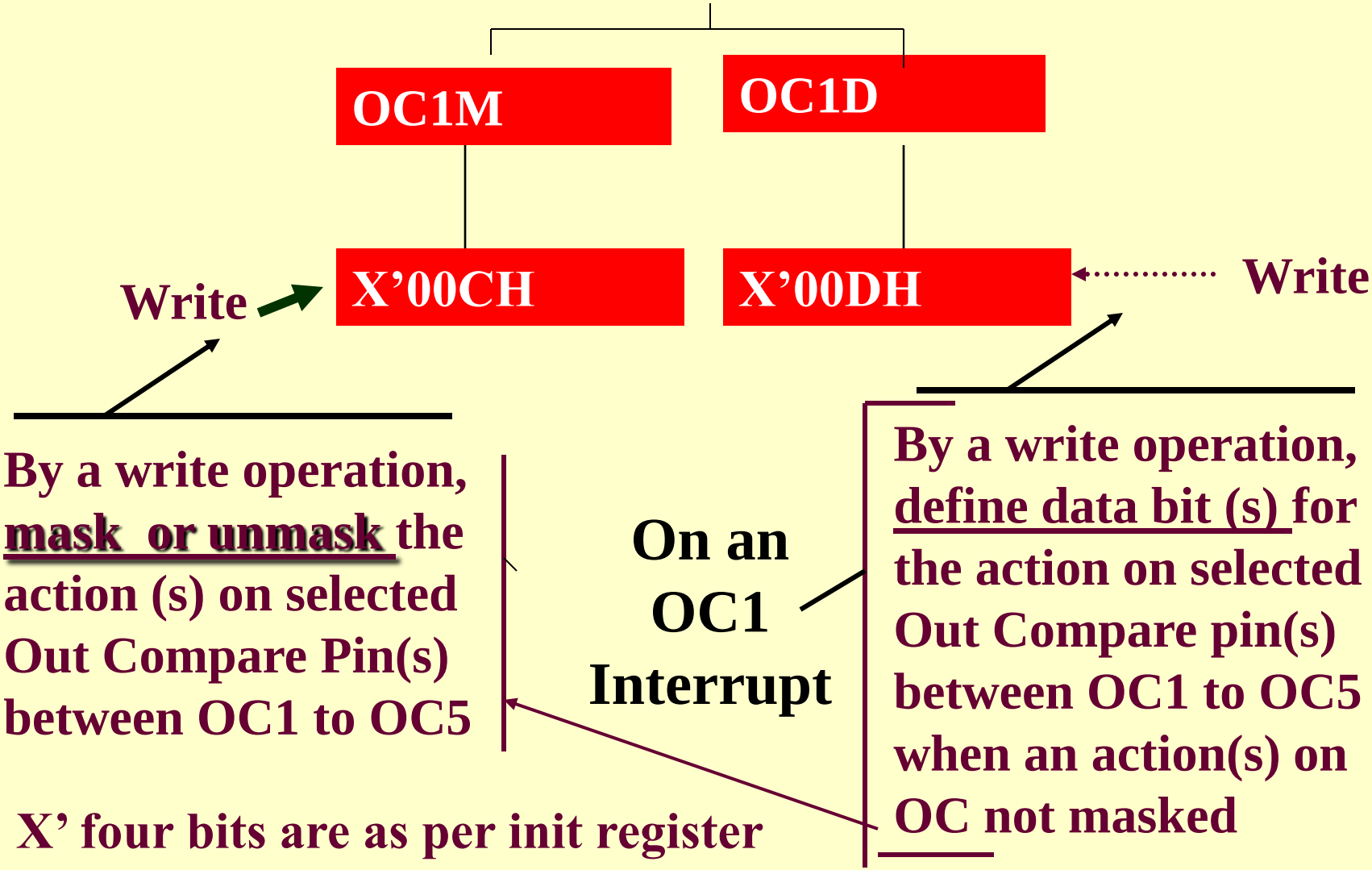
By a write operation, mask or unmask the interrupt_action (s) for a compare for the OC1 to OC5

OC5I,OC4I, OC3I, OC2I, OC1I bits at TMSK1

OC1 interrupt action on OC1 to OC5 Pins

OCx x = 1, 2, 3, 4, or 5 interrupt action on OC1 to OC5 Pins

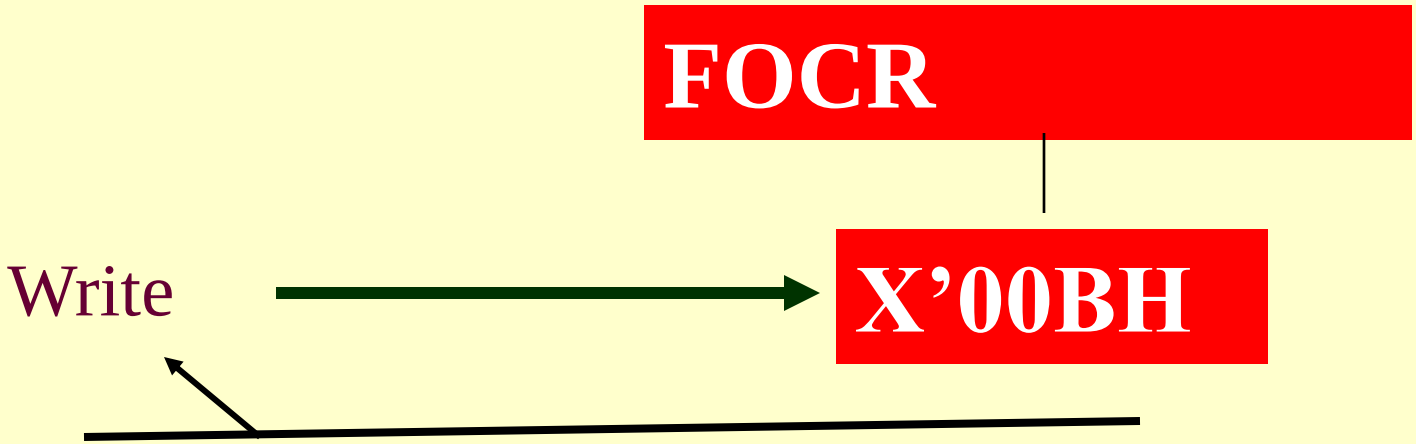
Mask for OC1 Action and OC1 Data for Action on equality of OC1D and x at TCNT



Force the change of all the 5 Outputs at the Out compare pins on action at OC1 (16 bit at OC1D = 16-bits x at TCNT)

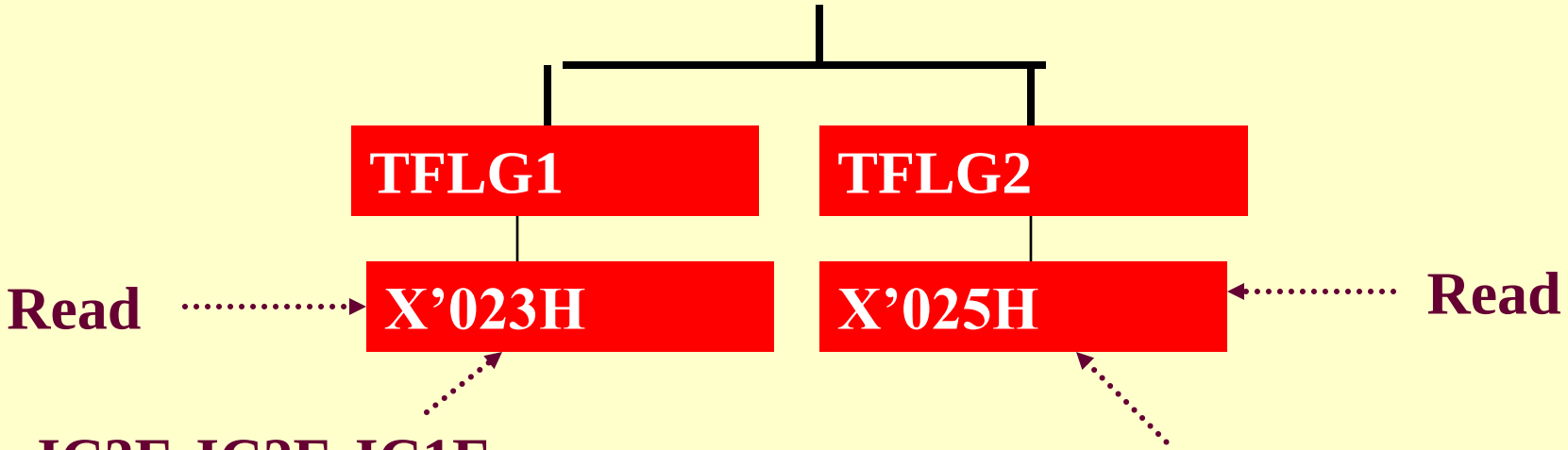
Step 1: Presetting of OC pin outputs

Step 2: Presetting Force Out Compare Register



By a write operation, **force** Out Compare Pins by OR operation of present bits with the 5 FOCR bits

Timer Flags for an IC or OC or *TCNT OV* or RTC or PACNT Input or PACNT OV Interrupt or Action Occurrences



IC3F, IC2F, IC1F, OC5F, OC4F, OC3F, OC2F, OC1F bits at TFLG1 at x'023H

PAIF, PAOVF, RTIF, *TOF* bits at TFLG2 at x'025H

X' four bits are as per init register

Write Registers for preset Timing Instance (s) at TCNT on an Out-Compare (s) output = 1 or 0 as per OLx bit 1 at pin between OC1 to OC5 pins

Summary

16-bit Timer Actions

- TCNT inputs, Reading and TCNT overflows
- 3 Input Captures
- Five Out-compares

We learnt

Timer Device registers and their addresses

- TCNT
- TIC1 to TIC3
- FOCR, OC1M, OC1D
- TOC1 to TOC5, TCTL1 and TCTL2
- TMSK1 and TMSK2
- TFLG1 and TFLG2

End of Lesson 5 on System Timing Devices – TCNT, ICs and OCs