Chapter 16

Motorola MC68HC11 Family MCU Architecture





On-Chip Memory Addresses

64 kB linear addressing space

68HC11/12

Address

IO, internal devices and system Control and status Registers

Internal RAM and ROM, RAM,EEPROM

On-Chip Memory Architecture

Internaldevices Registers **Data and Program**, constants, stored tables Common Memory

Address

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IO and internal devices Control and Status Registers

OPTION, COPRS, PPROG, IPRO, INIT, CONFIG, TESTI

Internal RAM and ROM, RAM,EEPROM

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| On-Chip Memory Addresses | | OPTION , |
|---------------------------------|---|------------------|
| 68HC11A8 | | COPRS, IPRO, |
| Address Space | IO and internal | INIT, |
| X'000H-34H - | Devices Registers | CONFIG, TESTI |
| X'039H-3FH | System Function Control Registers | |
| X'040H-FFH | | |
| B600H-7FFH - | 512kB EEPROM | |
| Е000Н- | 8 kB ROM | |
| FFFFH 2011 | Microcontrollers 2nd Ed. Raj Kamal Pearson Education | 6 |

| | <u>68HC11A8</u> |
|----------|-------------------------------------|
| Internal | 8kB ROM |
| | User Program, constants, |
| E000H- | stored tables |
| FEBFH | |
| | Interrupt Vectors |
| FEC0H- | |
| FFFBH | Reset vector (FFFC-FDH), |
| FEFCH- | Power-up reset vector (FFFE- |
| FFFFH | FFH) |

Memory Map 68HC11E9 64 kB address space **Address Space** IO and internal **X'000H-FFH** → **Devices, and System Registers** and Internal RAM **X000H-FFH** → Internal RAM addressable by **8-bit as the Registers Off-chip** addresses → 53 kB External ROM/RAM **B600H-7FFH** → Internal EEPROM **D000H-Internal 12kB ROM** X' and X eight bits are as per init register -IS-... 2110 Ed. Nai Kama 2011

Summary

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We learnt

- On-Chip Memory Addresses
- Memory Map

Memory Map

- IO/Devices Control and Status Registers
- 192-byte Internal RAM
- Internal ROM
- Internal EEPROM
- External ROM/RAM

End of Lesson 3 on Memory

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