Chapter 16

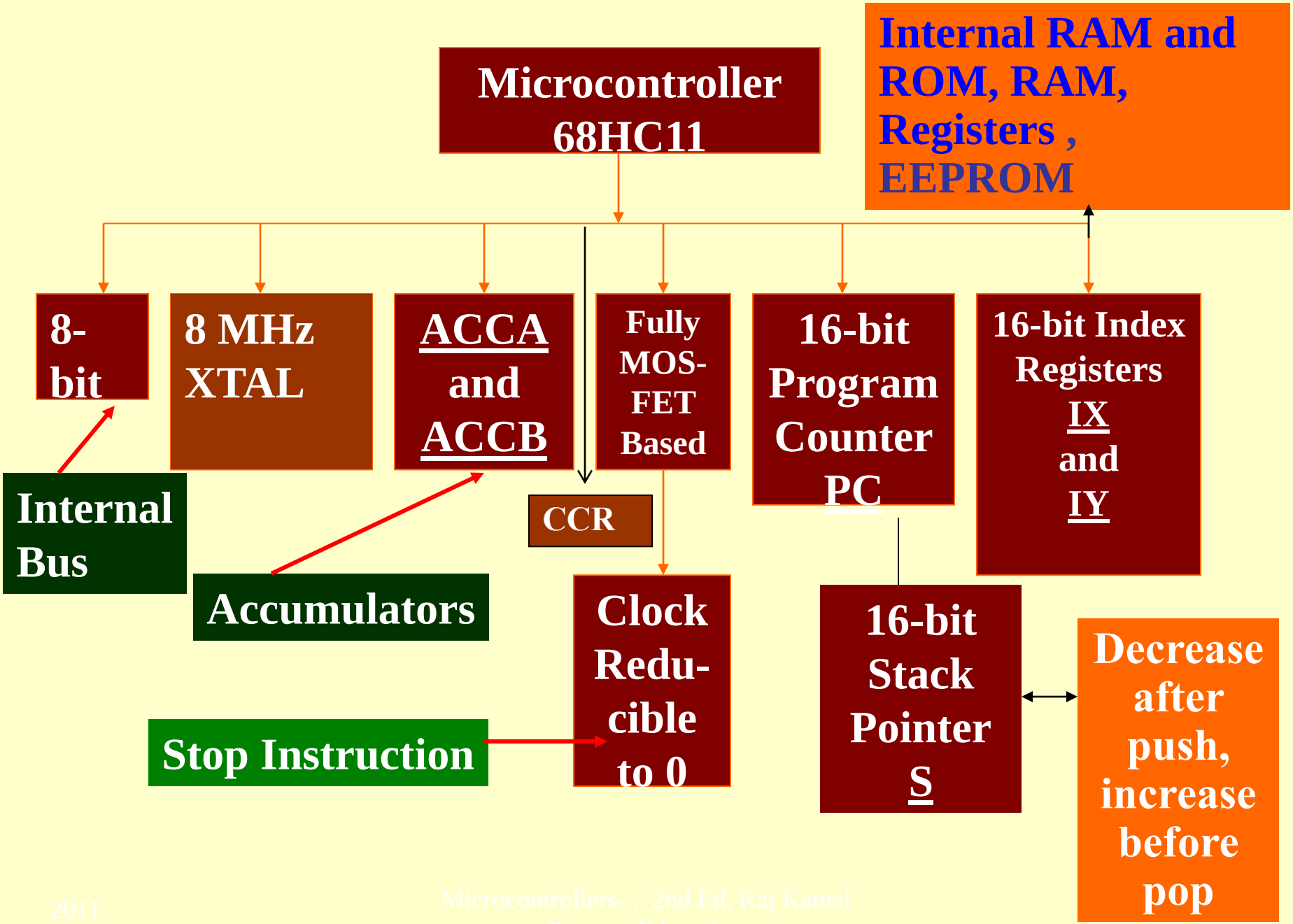
Motorola MC68HC11 Family MCU Architecture

Lesson 1

68HC11 MCU Architecture overview

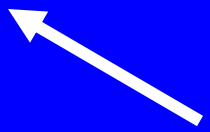
CPU Registers

- ACCA and ACCB
- 16-bit Program Counter PC
- 16-bit Stack Pointer S
- 16-bit Index Registers IX and IY
- 8- bit CCR (Condition Code Register)


Microcontroller 68HC11
Internal RAM and ROM, RAM, Registers , EEPROM
8-bit
8 MHz XTAL
ACCA and ACCB
Fully MOS-FET Based
16-bit Program Counter PC
16-bit Index Registers IX and IY
Internal Bus
Accumulators
CCR
Clock Redu-cible to 0
16-bit Stack Pointer S
Decrease after push, increase before pop
Stop Instruction

MCU Architecture overview

- Fully static operation- MCU clock can be reduced to 0 – being fully MOSFETs based



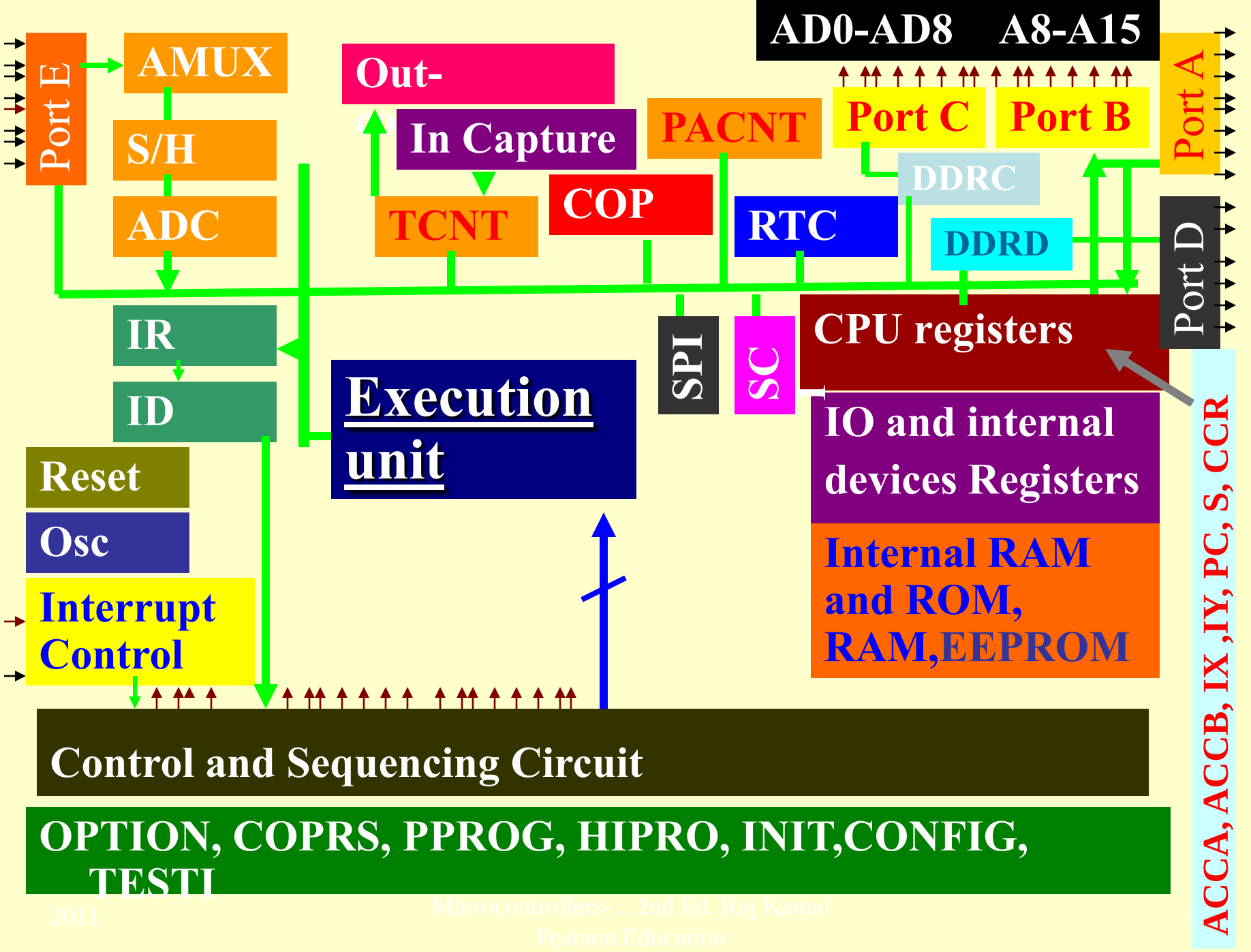
Stop Instruction

Performance

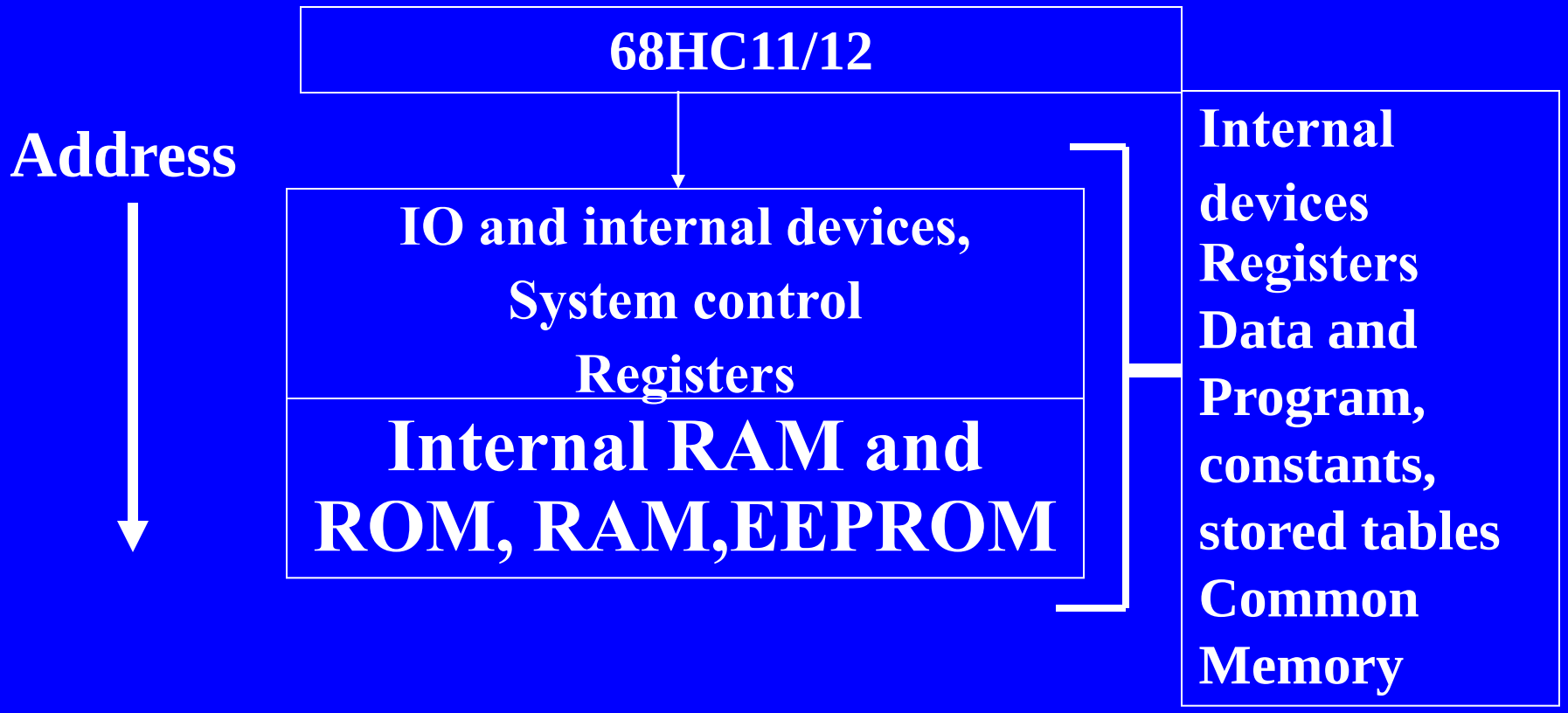
As per 8MHz XTL 2MHz E-Clock

- 68HC11 common 8-bit internal bus for the 16-bit addressing and 8-bit data
- Princeton architecture bus
- Bus interface for 8-bit data and instructions.
- Two interrupts – Maskable Interrupt request (IRQ) and Initialization option as unmaskable (XIRQ)
- PC initialization using reset vector FFFEH-FFEFH

68HC11 Architecture Overview

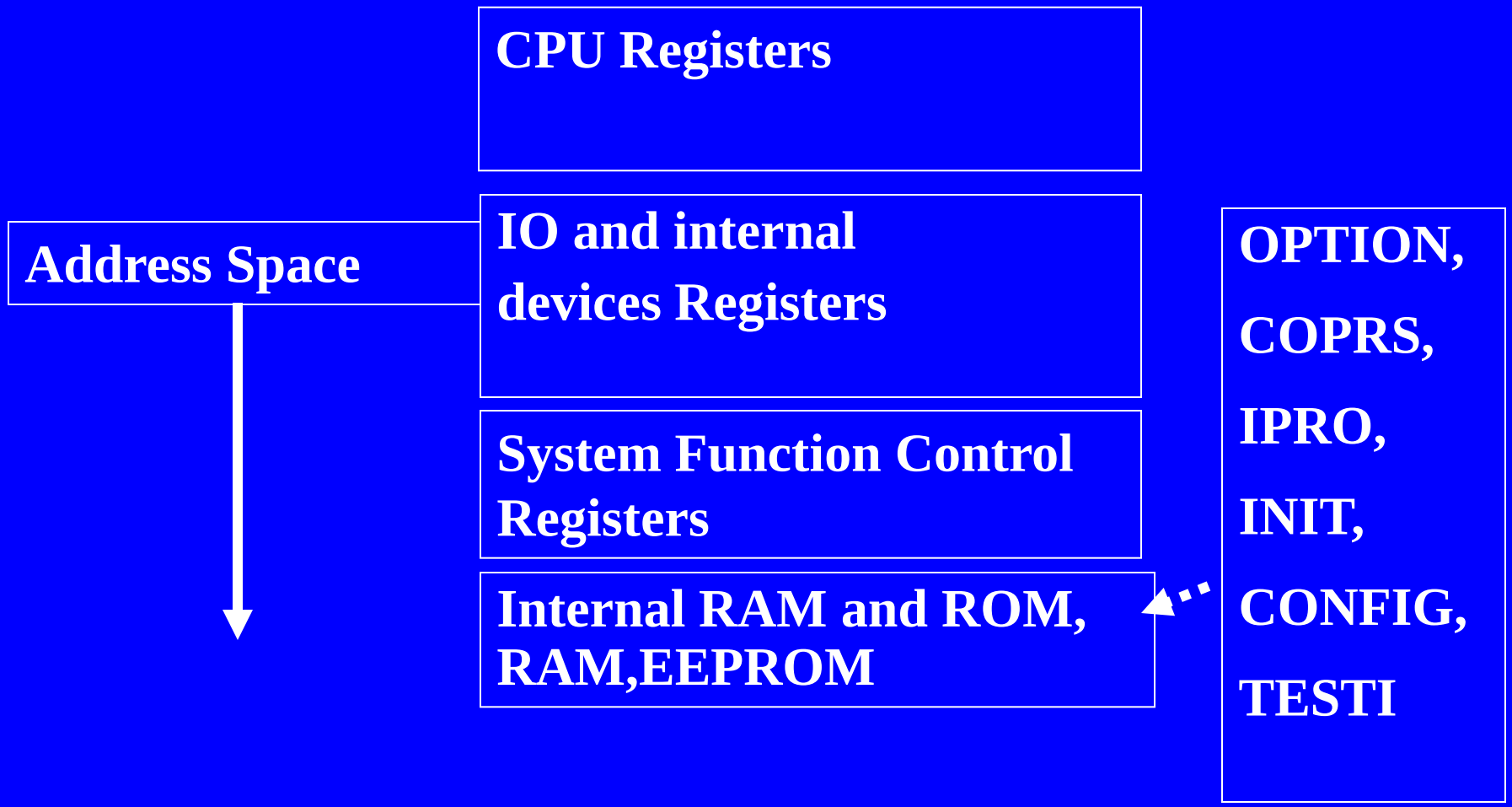

AD0-AD8 A8-A15
Port E
AMUX
S/H
ADC
Out-
In Capture
TCNT
COP
PACNT
Port C
Port B
Port A
DDRC
DDRD
RTC
Port D
IR
ID
Execution unit
SPI
SC
CPU registers
IO and internal devices Registers
Internal RAM and ROM, RAM,EEPROM
Reset
Osc
Interrupt Control
Control and Sequencing Circuit
OPTION, COPRS, PPROG, HIPRO, INIT,CONFIG, TESTI
ACCA, ACCB, IX ,IY, PC, S, CCR

64 kB of linear address space



Memory Architecture

68HC11 Family Programming Model



68HC11 Family Programming Model

- Instructions have **8** data type
- Few use 16- bit data types
- Processor operation of 16-bit data type is as per word alignment at memory in *big endian* [least significant byte stored as higher bits (address 1) of a word]

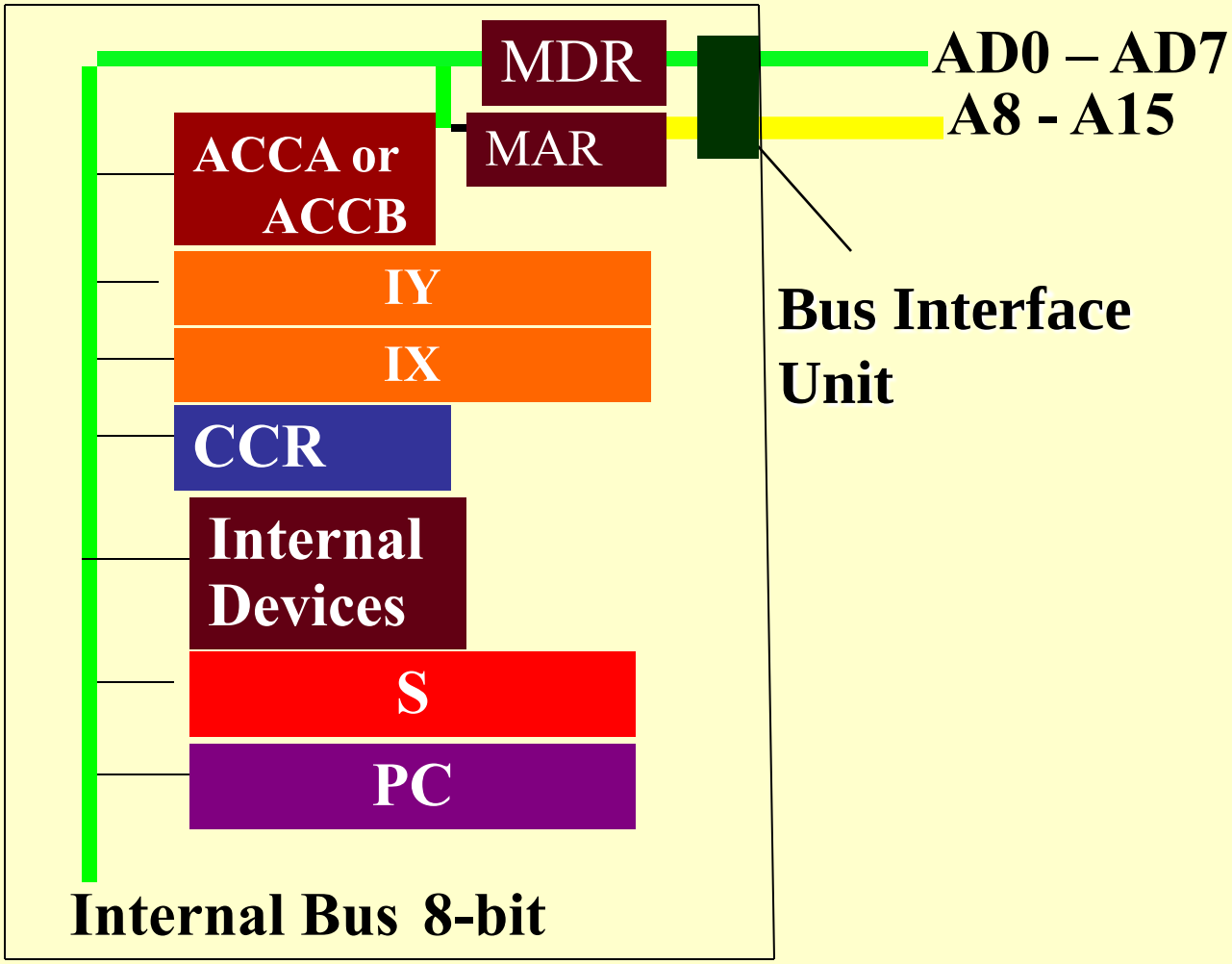
16-bit word alignment

A 16bit word in memory

Big Endian	Address
Byte1 (MSB)	Address0
Byte0 (LSB)	Address1

68HC11 Address and Data Buses

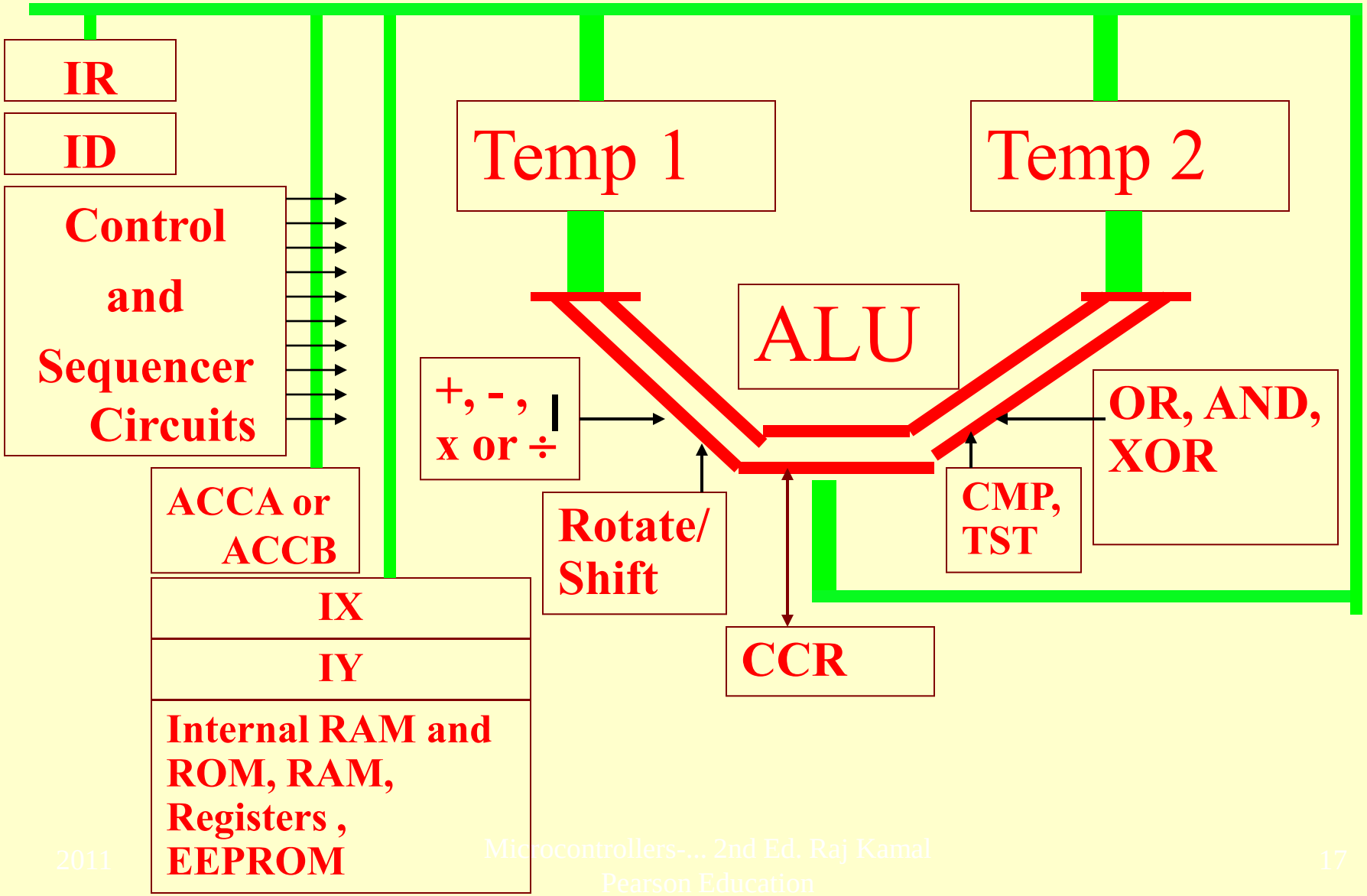
Internal and External Buses



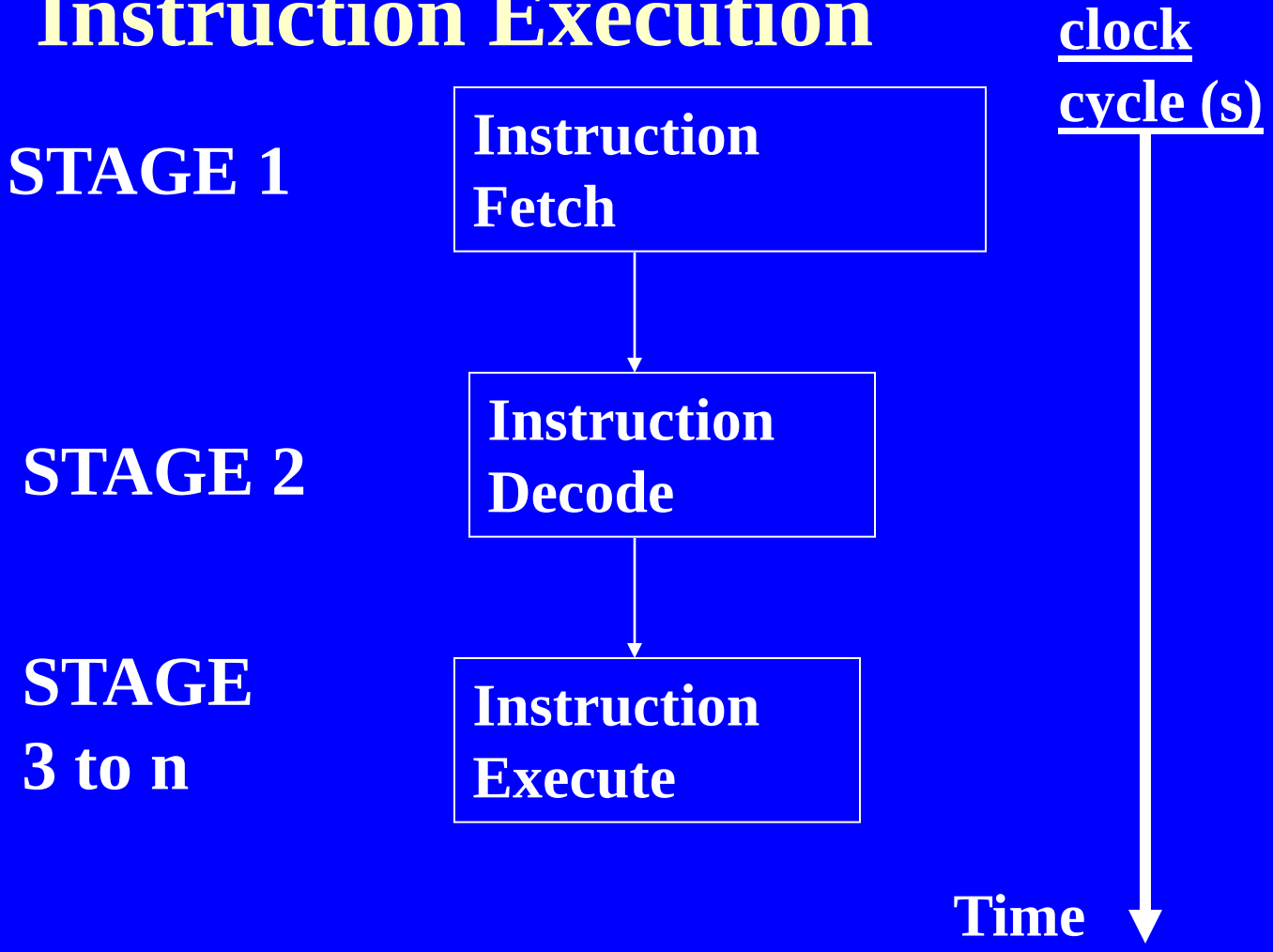
Execution Unit- ALU

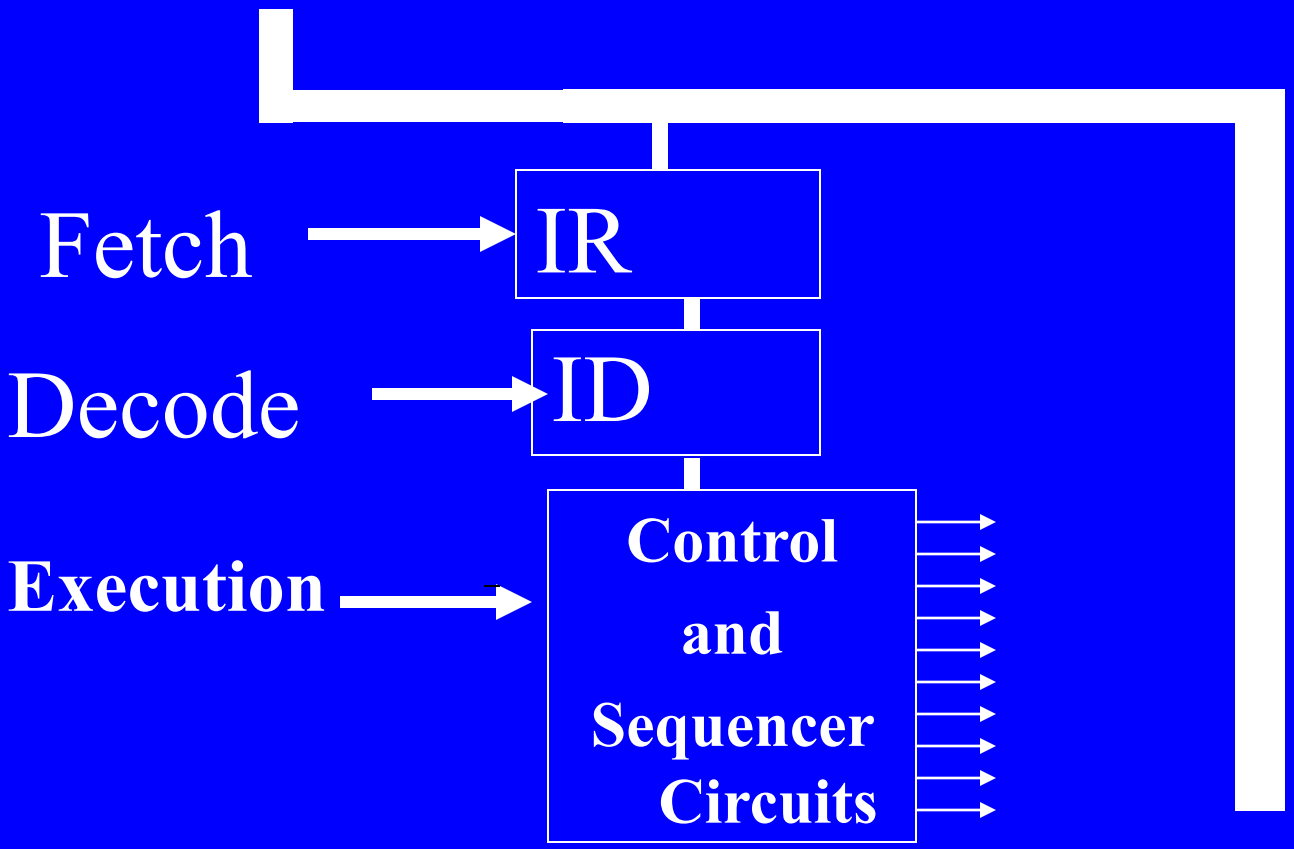
- ACCA or ACCB used as 8-bit ACC or as16-bit ACCD (double accumulator)
- 8-bit ALU includes *multiplier* and *divide*

Execution Unit

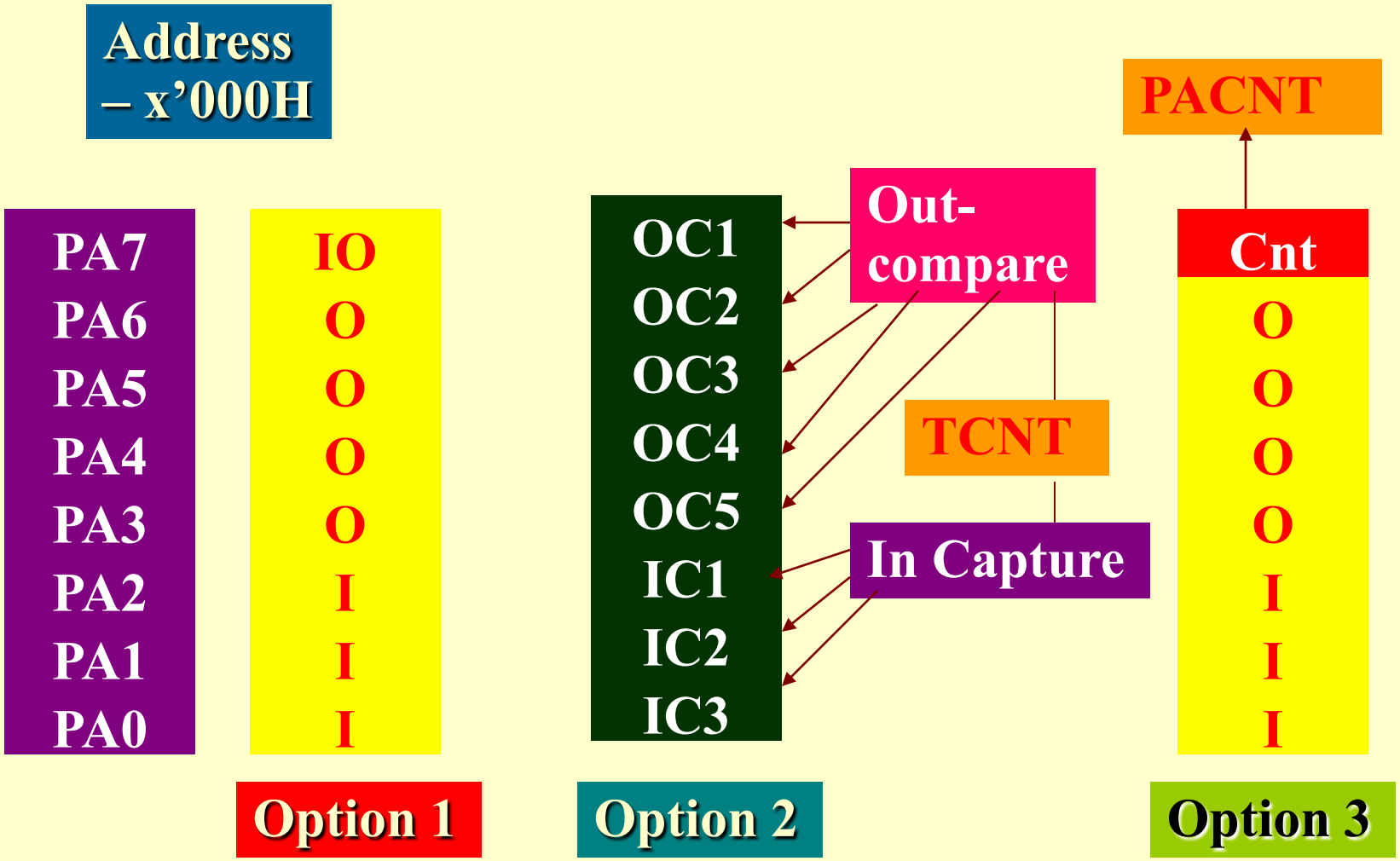


Instruction Execution



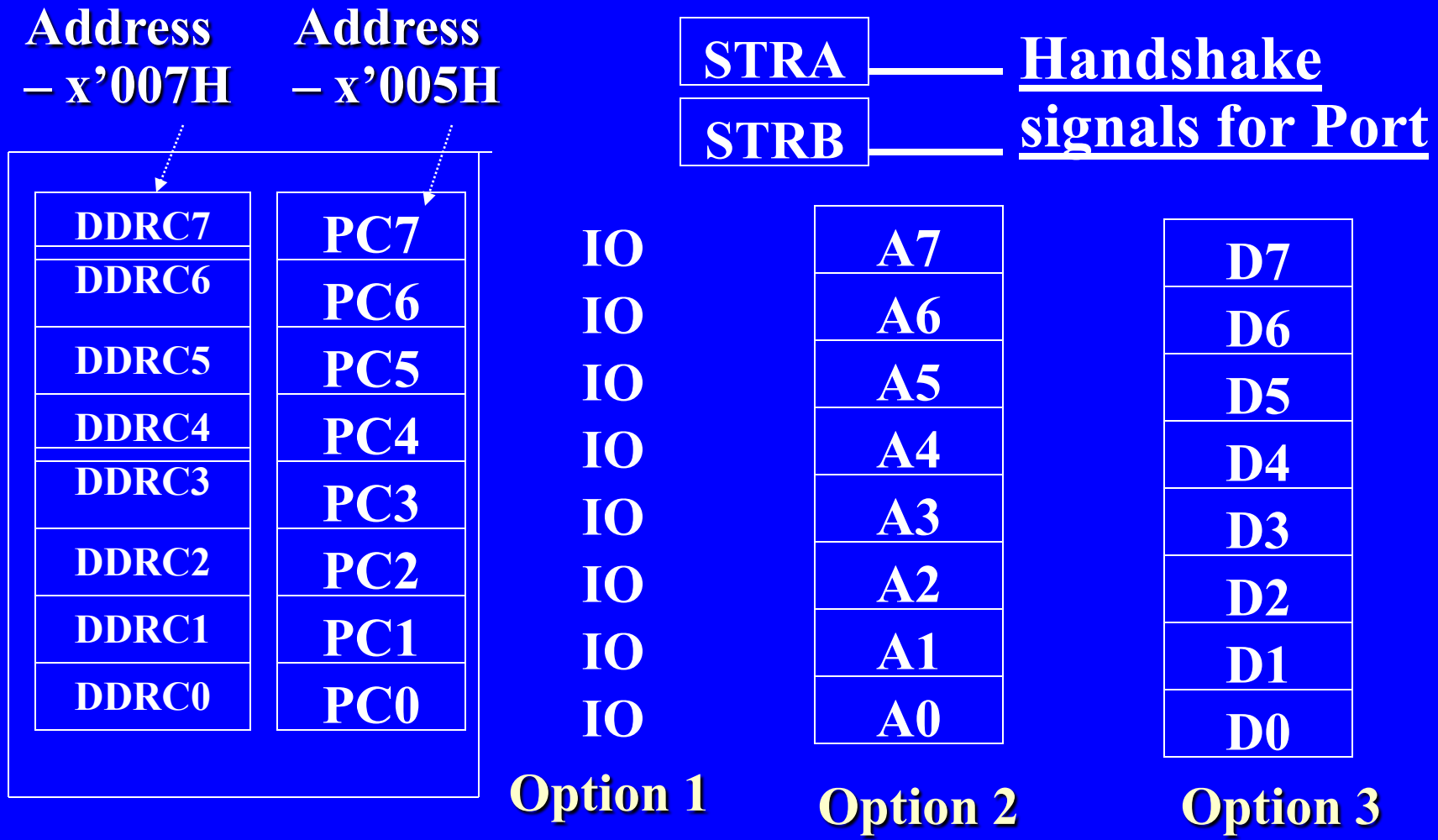


Control memory micro codes based - Implementation


Address – x'000H
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
IO
O
O
O
O
I
I
I
Option 1
OC1
OC2
OC3
OC4
OC5
IC1
IC2
IC3
Out-compare
TCNT
In Capture
Option 2
PACNT
Cnt
O
O
O
O
I
I
I
Option 3

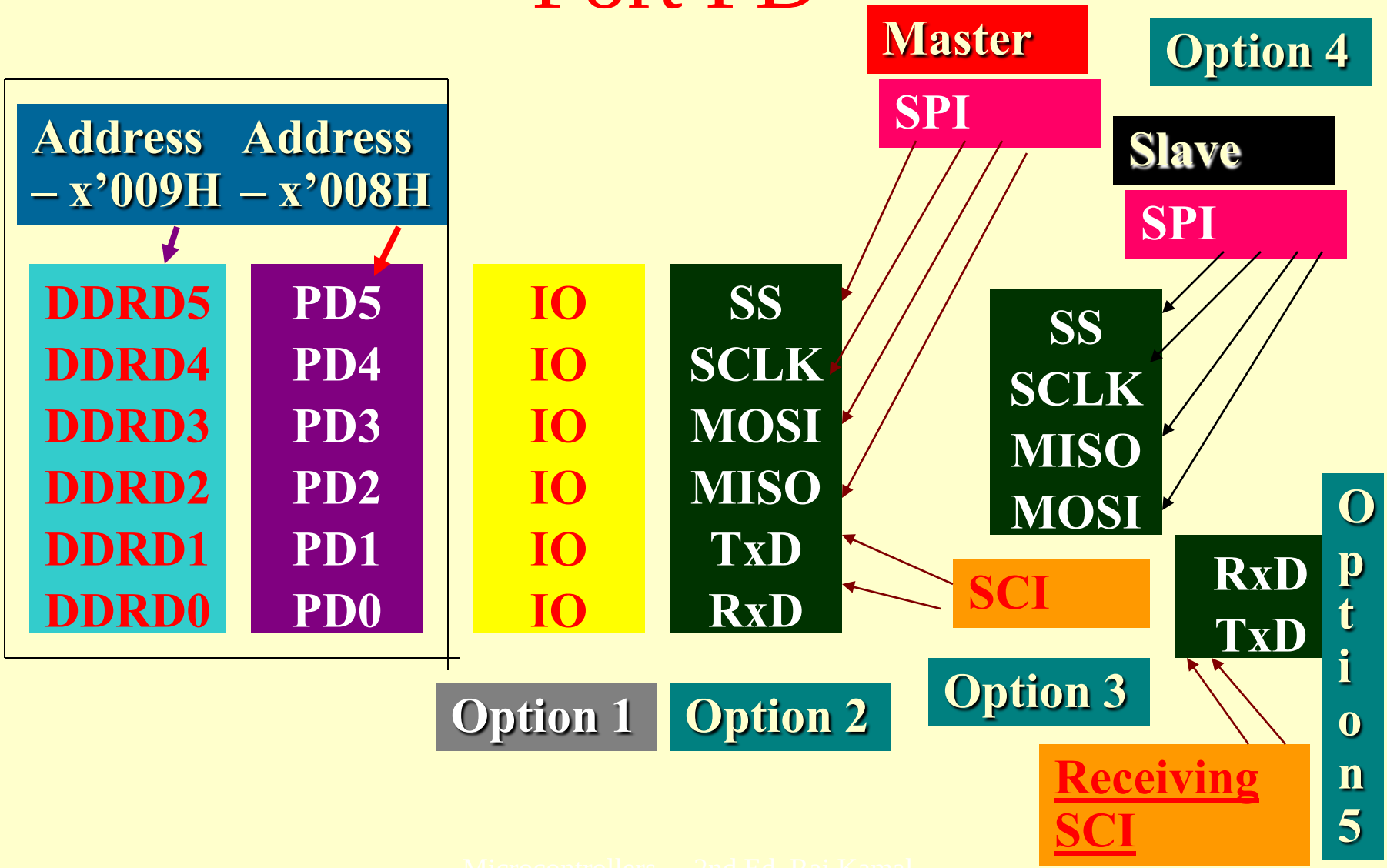
Port PB

Address – x'004H

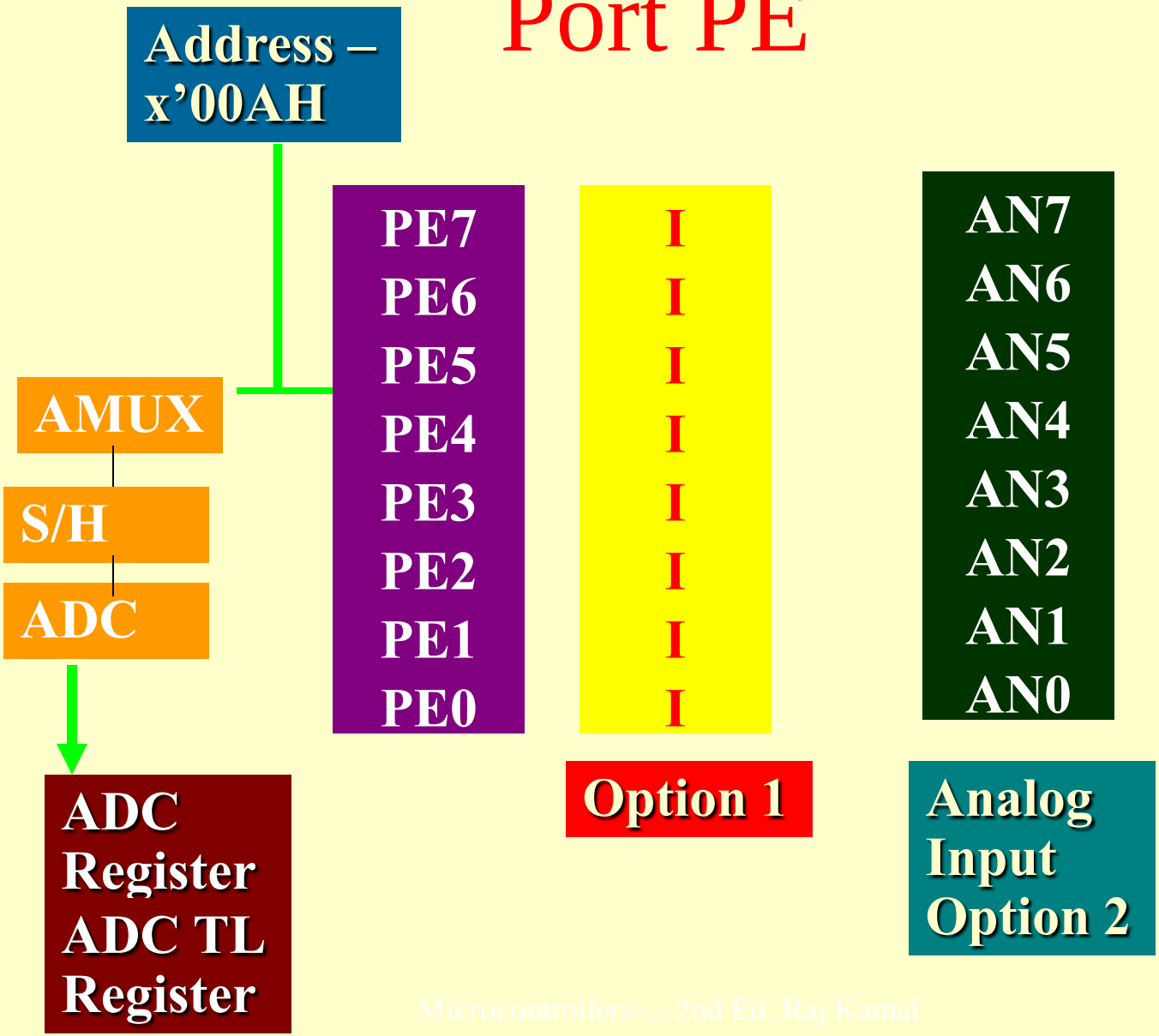

Address – x'007H
Address – x'005H
DDRC7
DDRC6
DDRC5
DDRC4
DDRC3
DDRC2
DDRC1
DDRC0
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
STRA
STRB
Handshake signals for Port
IO
IO
IO
IO
IO
IO
IO
IO
Option 1
A7
A6
A5
A4
A3
A2
A1
A0
Option 2
D7
D6
D5
D4
D3
D2
D1
D0
Option 3

Port PC

Port PD


Address – x'009H
Address – x'008H
DDRD5
DDRD4
DDRD3
DDRD2
DDRD1
DDRD0
PD5
PD4
PD3
PD2
PD1
PD0
IO
IO
IO
IO
IO
IO
SS
SCLK
MOSI
MISO
TxD
RxD
Option 1
Option 2
Master
SPI
Option 4
Slave
SPI
SS
SCLK
MISO
MOSI
SCI
RxD
TxD
Option 3
Receiving SCI
Option 5

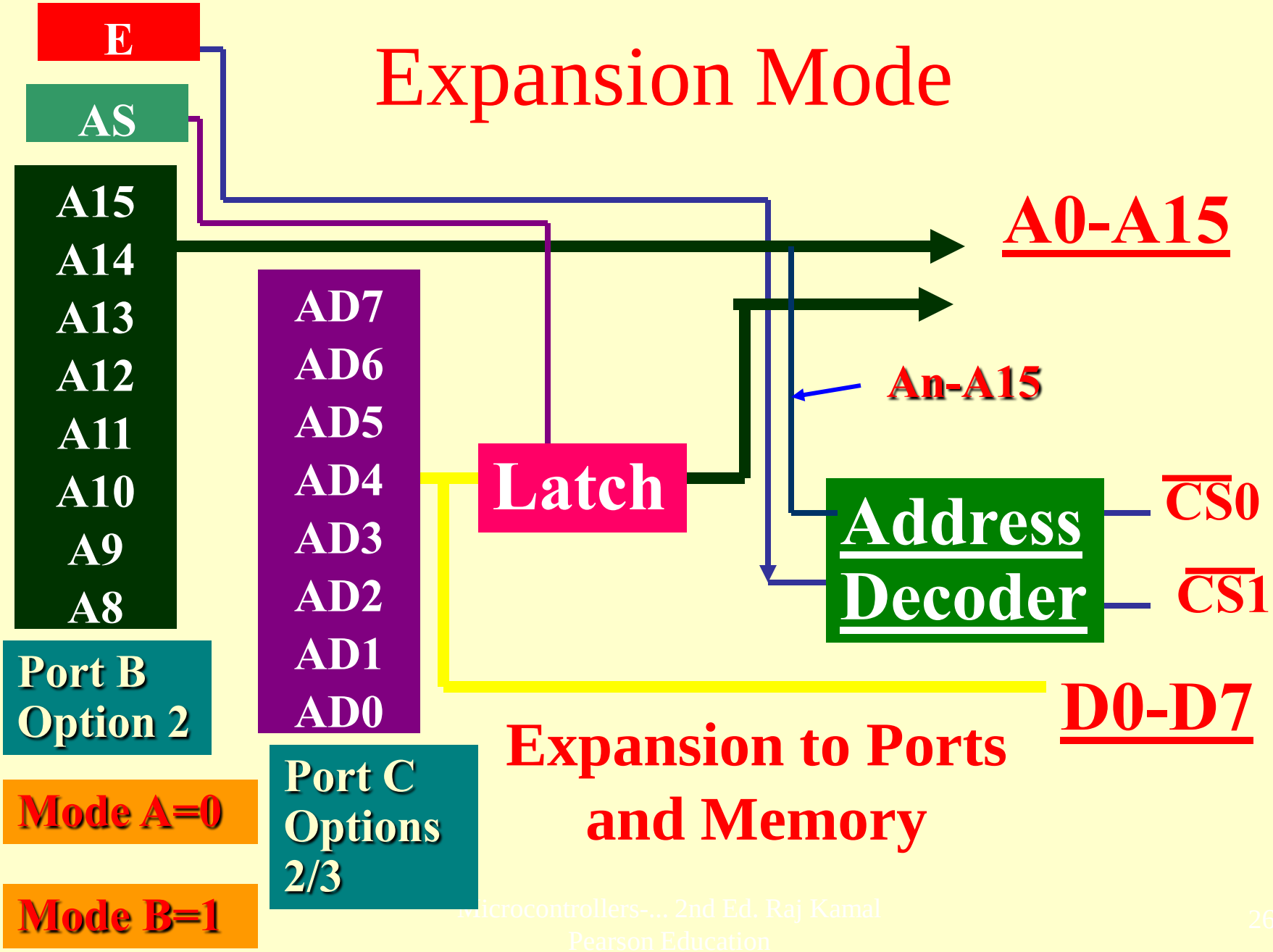
Port PE


Address – x'00AH
PE7
PE6
PE5
PE4
PE3
PE2
PE1
PE0
I
I
I
I
I
I
I
I
AN7
AN6
AN5
AN4
AN3
AN2
AN1
AN0
AMUX
S/H
ADC
ADC Register
ADC TL Register
Option 1
Analog Input Option 2

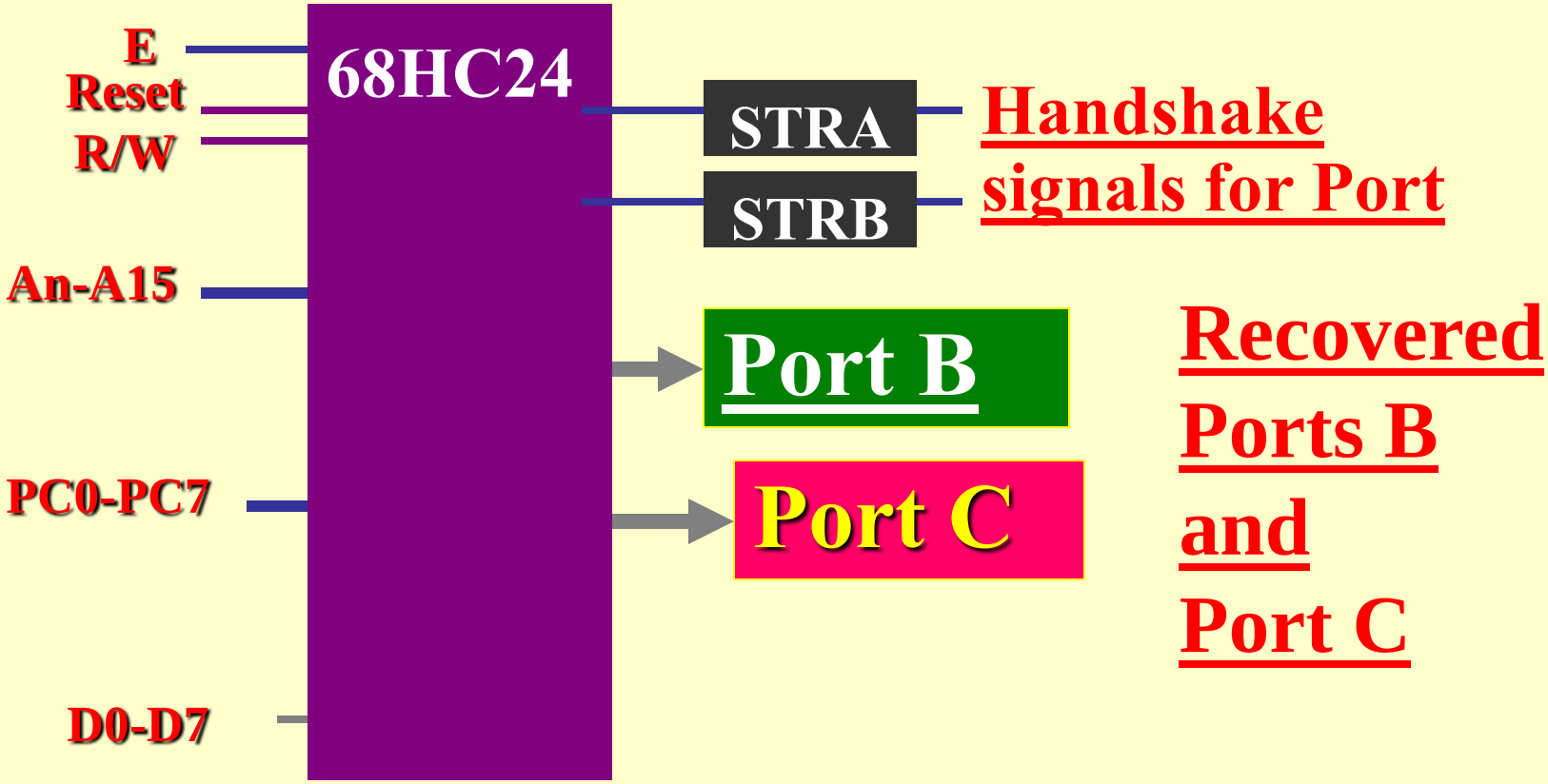
Expansion Mode

- Expanded Mode used for interfacing External Memory and Ports
- Expanded Mode looses Port B and Port B
- Recovered back by using 68HC24

Expansion Mode



Lost Ports Replacement Unit



Mode A=0

Mode B=1

Summary

We learnt

- 68HC11 family 8-bit processor
- PC, S, ACCA, ACCB, IX, IY, CCR
- Princeton architecture
- 8 bit data type
- Big endian 16-bit word alignment
- Two interrupts – Maskable Interrupt request ($\overline{\text{IRQ}}$) and Initialization option as unmaskable ($\overline{\text{XIRQ}}$)
- PC initialization using reset vector

We learnt

Internal and External Memory Addresses-

- IO/Devices Control and Status Registers
- System Function Control Registers
- Internal RAM
- Internal ROM
- EEPROM

We learnt

Internal Devices

- TCNT with out compare, input capture,
- SPI, SCI
- RTC
- PACNT
- Port E with option of analog inputs multi channel AMUX, S/H, ADC

We learnt

Internal Devices

- Port B /A8-A15,
- Port C with DDRC / AD0-AD7/
- Port A /IC1-IC3, OC1-OC5
- Port D with DDRD/SCI/SPI Master/Slave

End of Lesson 1 on MCU Architecture overview