Chapter 15

ARM – Architecture, Programming and Development Tools

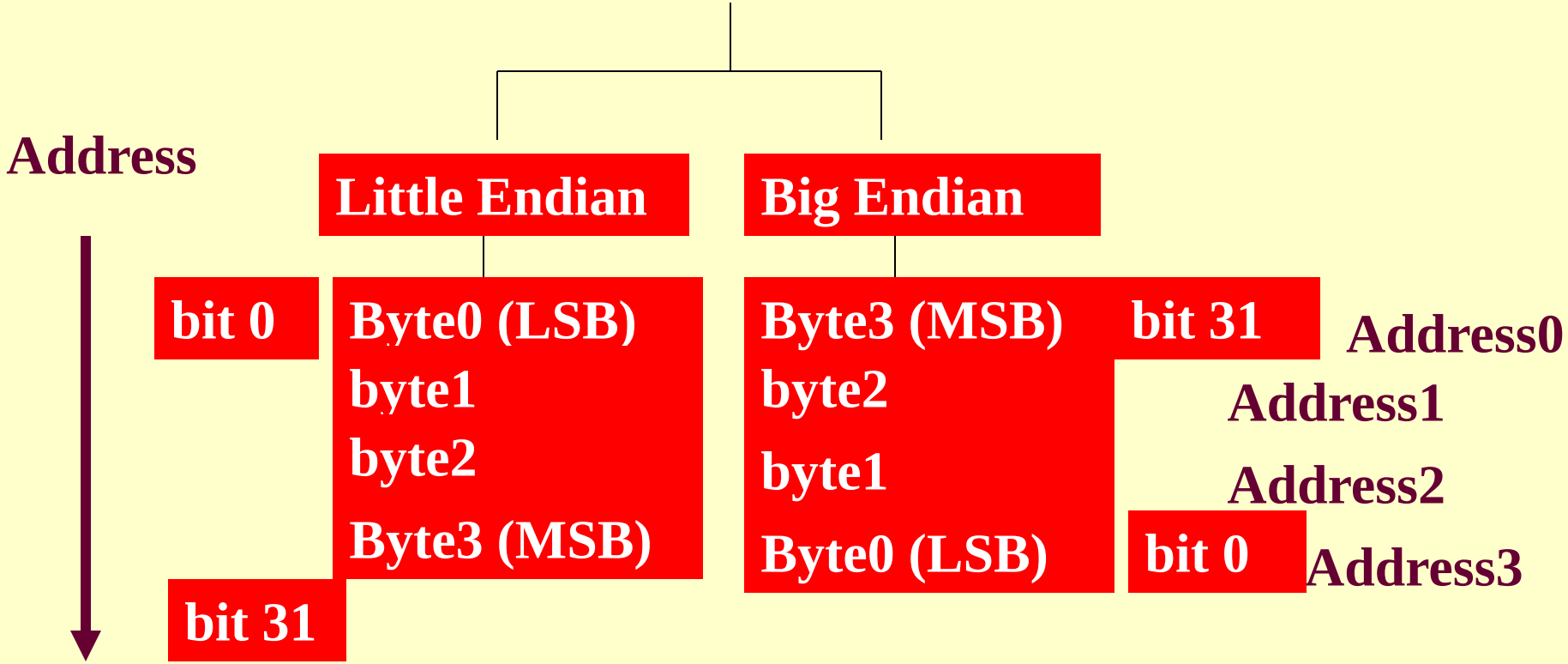
Lesson 3

ARM Programming Model

ARM data types

- Word is 32 bits long.
- Word can be divided into four 8-bit bytes.
- ARM addresses cam be 32 bits long.
- Address refers to byte.
  - Address 4 starts at byte 4.
- Can be configured at power-up initialisation as either little- or bit-endian mode.

A 32bit word Endianness



Two Initialization options

- Registers

R0 R1 R2 R3 R4 R5 R6 R7 Lo registers

R8 R9 R10 R11 R12 Hi registers

SP (R13) Stack Pointer

LR (R14) Link Register

PC (Rr15) Program Counter

CPSR

N (negative), Z (zero), C (carry), V (overflow).

Every arithmetic, logical, or shifting operation sets CPSR bits

SPSR

ARM data types in Programming

- Word 32 bits long
- Half Word 16-bit long
- Byte 8-bit long

ARM status bits

- Every arithmetic, logical, or shifting operation sets CPSR bits:
  - N (negative), Z (zero), C (carry), V (overflow).
- Examples:
  - -1 + 1 = 0: NZCV = 0110.
  - 2^{31}-1+1 = -2^{31}: NZCV = 0101.

ARM Family Programming Model

- 16 general-purpose registers with program counter as one of the register (R15)

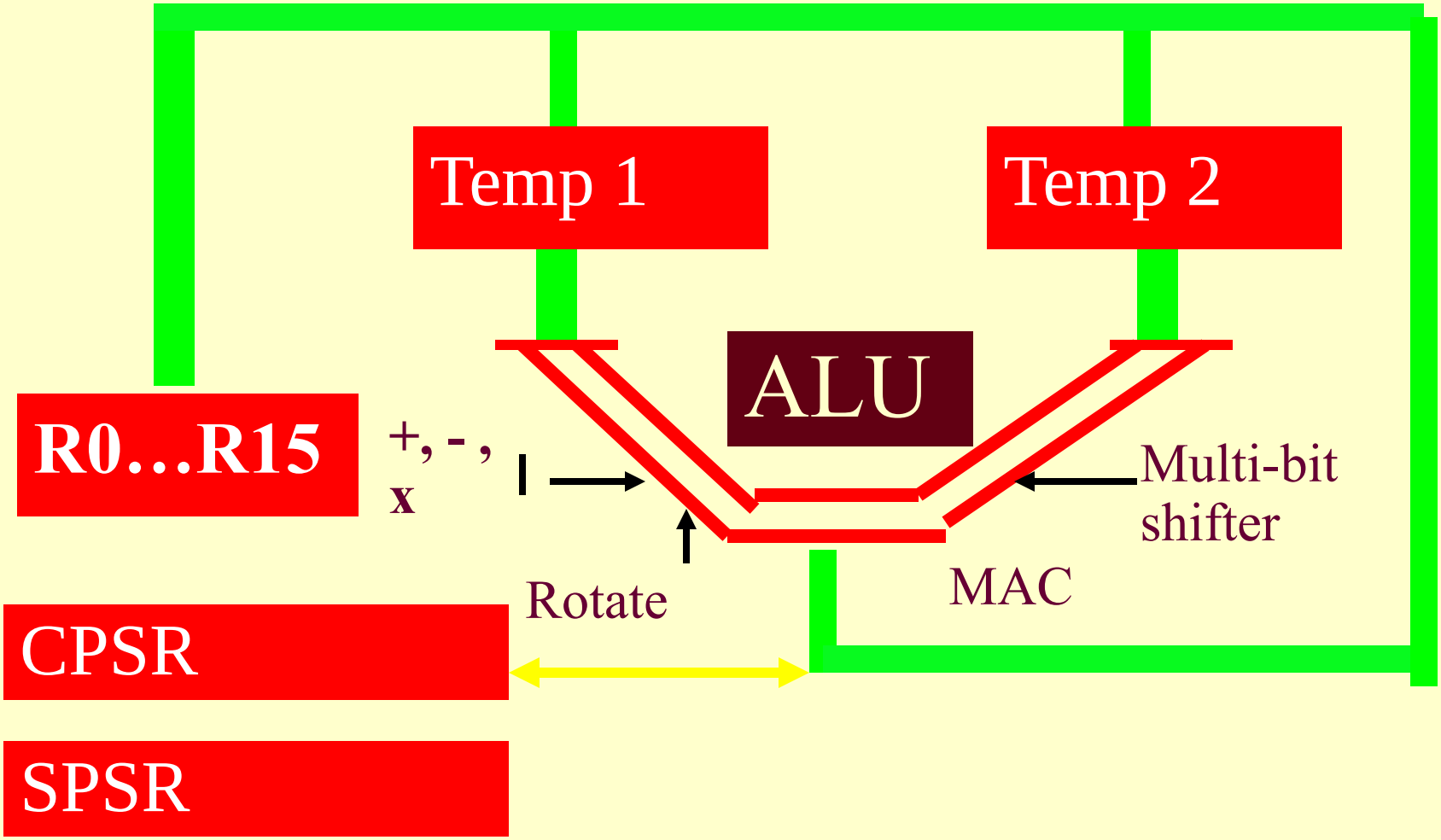
CPSR and SPSR

- CPSR (Conditions and Processor Status Register)
- SPSR (Saved Program Status Register) Saves Program Status Register from CPSR on branch and link (routine call) and SPSR can be stacked for each processor mode

Register ALU

- 32-bit RALU and high-performance multiplier
- Instructions have 8-, 16-, and 32-bit data types

RALU


Temp 1
Temp 2
ALU
R0…R15
+, - , x
Multi-bit shifter
Rotate
MAC
CPSR
SPSR

ARM 7 T Variants

ARM® TDMI ™ **instruction set** options-

1. High-performance 32-bit instruction set-
2. High-code-density Thumb®16-bit instruction set than 32-bit instruction architecture

Summary

We learnt

- 32 bit Sixteen Registers plus CPSR and SPSR
- 32/16/8 bit data types
- r15 Program counter
- r14 Link Register for return
- r13 stack pointer

End of Lesson 3 on ARM Programming Model