Chapter 15

ARM – Architecture, Programming and Development Tools

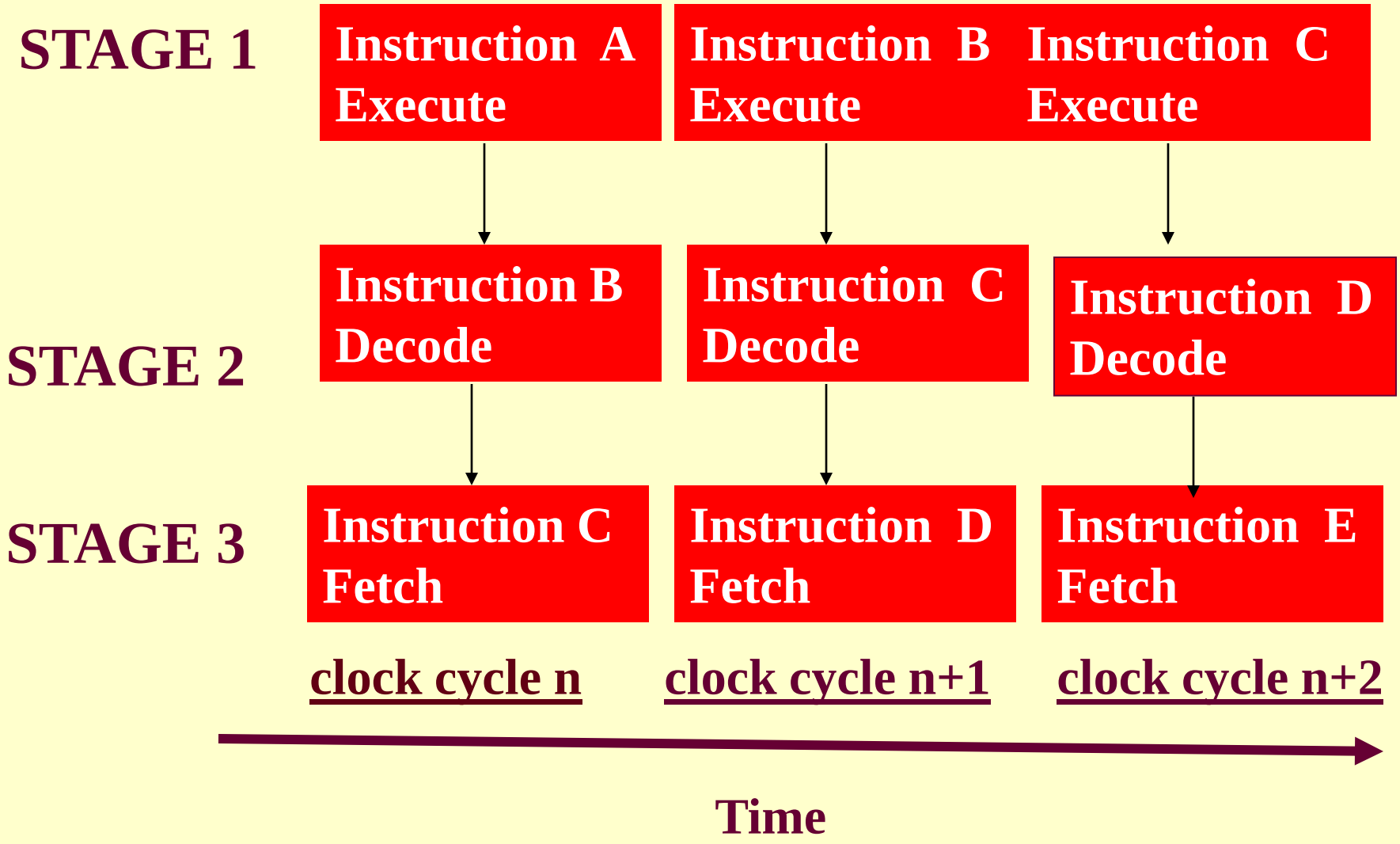
Lesson 2

ARM7 Architecture

ARM7TDMI

- Design centers around and concentrate on simple instructions
- Smaller and simpler processor circuit, Simpler decoding sub-unit.
- Lower power– more space for other performing units

A three stage pipeline



Pipeline

- Three stage Pipelining in superscalar processor facilitating each instruction fetch is in single cycle, decoding in single cycle and execute in the single cycle: Three times execution speed boost up

Buses

- ARM 7 common internal bus for the address and data of 32-bit in-32-bit Princeton architecture bus and bus interface for 32-bit data and instructions.
- ARM9 - Harvard Architecture.

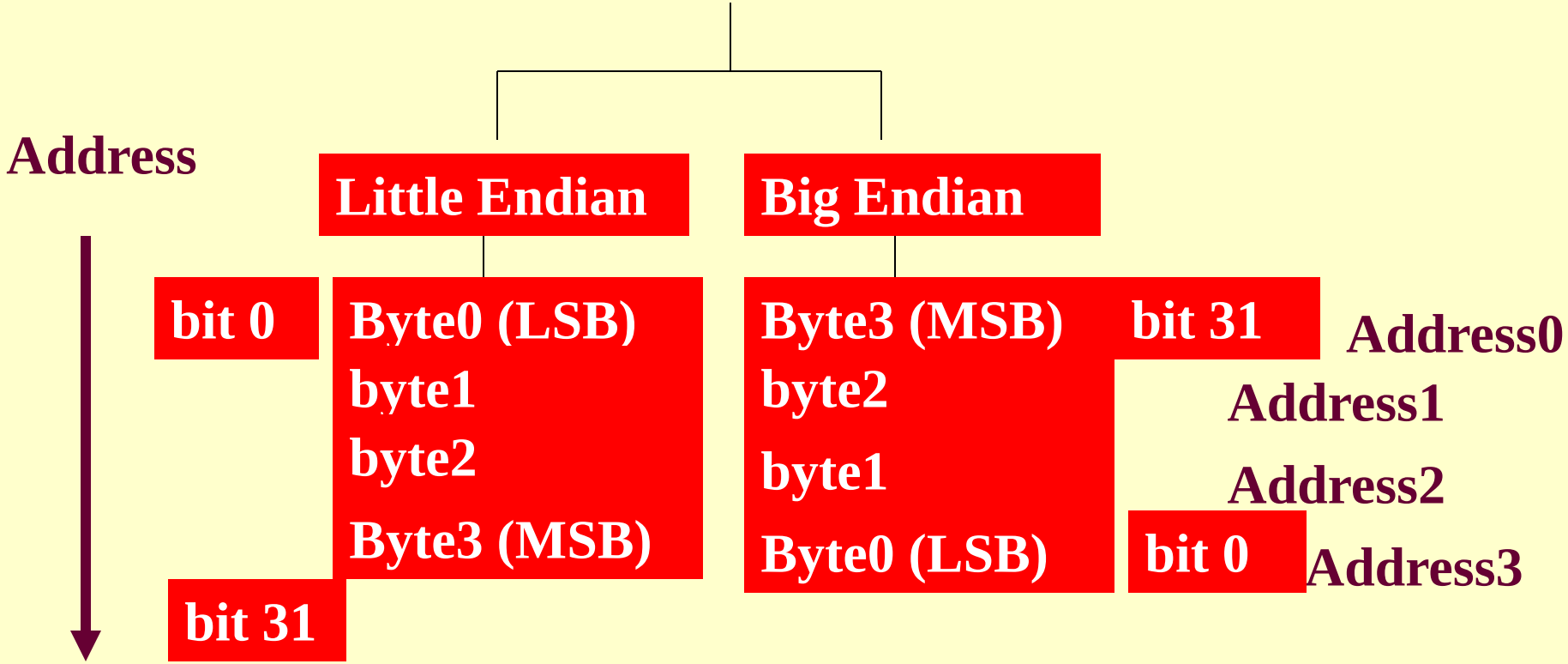
ARM 7 architecture

- Uses 0.25µm and less die size HCMOS technology
- Very small die size facilitating low voltage operations and low power consumption
- Very small power consumption means very low MIPS/Watt

ARM 7 architecture

- Processor operation on the words *as per initialization*. A word alignment can then be in *big endian* [least significant byte stored as higher bits (address 3) of a word] or *little endian* [least significant byte stored as lower bits (address 0) of a word].

A 32bit word



Two Initialization options

ARM 7 architecture

- Fully static operation- MCU clock can be reduced to 0 and since fully MOSFETs based

ARM 7 architecture

- Optimized for fast interrupts and DSP algorithms
- There are two types of requests for interrupts- Fast interrupt request (FIQ) and interrupt request (IRQ). Fast means high priority.
- 4 gigabytes of linear address space

ARM 7 architecture

- 32-bit large set of 16 general-purpose registers with program counter as one of the register (r15) plus CPSR and SPSR -are two other registers.

Features

- Coprocessor interface to connect coprocessors, like DSP processors and Java Accelerators

Features

- System control functions implemented in standard low-power logic
- Cost-effective, compact chip

ARM 7 T Variants

ARM® TDMI ™ instruction set options-

1. High-performance 32-bit instruction set-
2. High-code-density Thumb®16-bit instruction set than 32-bit instruction architecture

Summary

We learnt

- 32 bit Sixteen Registers plus CPSR and SPSR
- ARM 9 and ARM7 Harvard and Princeton architectures
- Initialized options: little or big endian modes

We learnt

- 32/16/8 bit data types
- Two interrupts - Fast interrupt request (FIQ) and interrupt request (IRQ)

End of Lesson 2 on ARM7 Architecture