Chapter 15

ARM – Architecture, Programming and Development Tools

Lesson 1

ARM CPUs

ARM

From ARM RISC Machines

Embedded RISC Core ARM7TDMI (http://www.arm.com/news/5135.html)

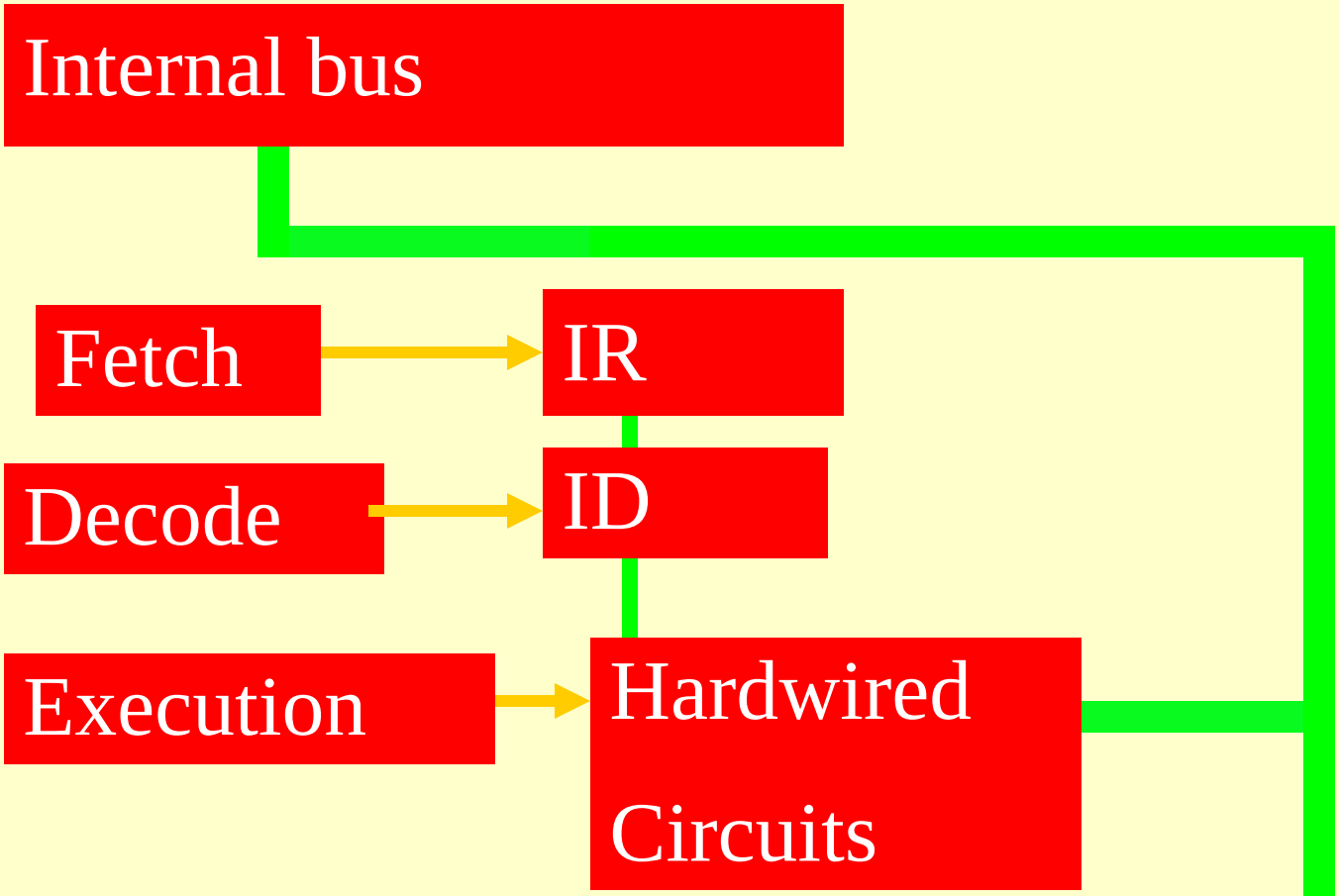
- ARM family of general-purpose 32-bit microprocessors offers *high performance* and *very low MIPS/watt power consumption*
- 32-bit RISC architecture

RISC Features

- **Reduced instruction set computer**
- **Same Length instructions**
- **Single Cycle Execution (most instructions) and thus high-performance by pipelining and superscaling**

RISC Features

- Hardwired implementation of Instructions
- Large Register Set(s)
- Load and Store Architecture

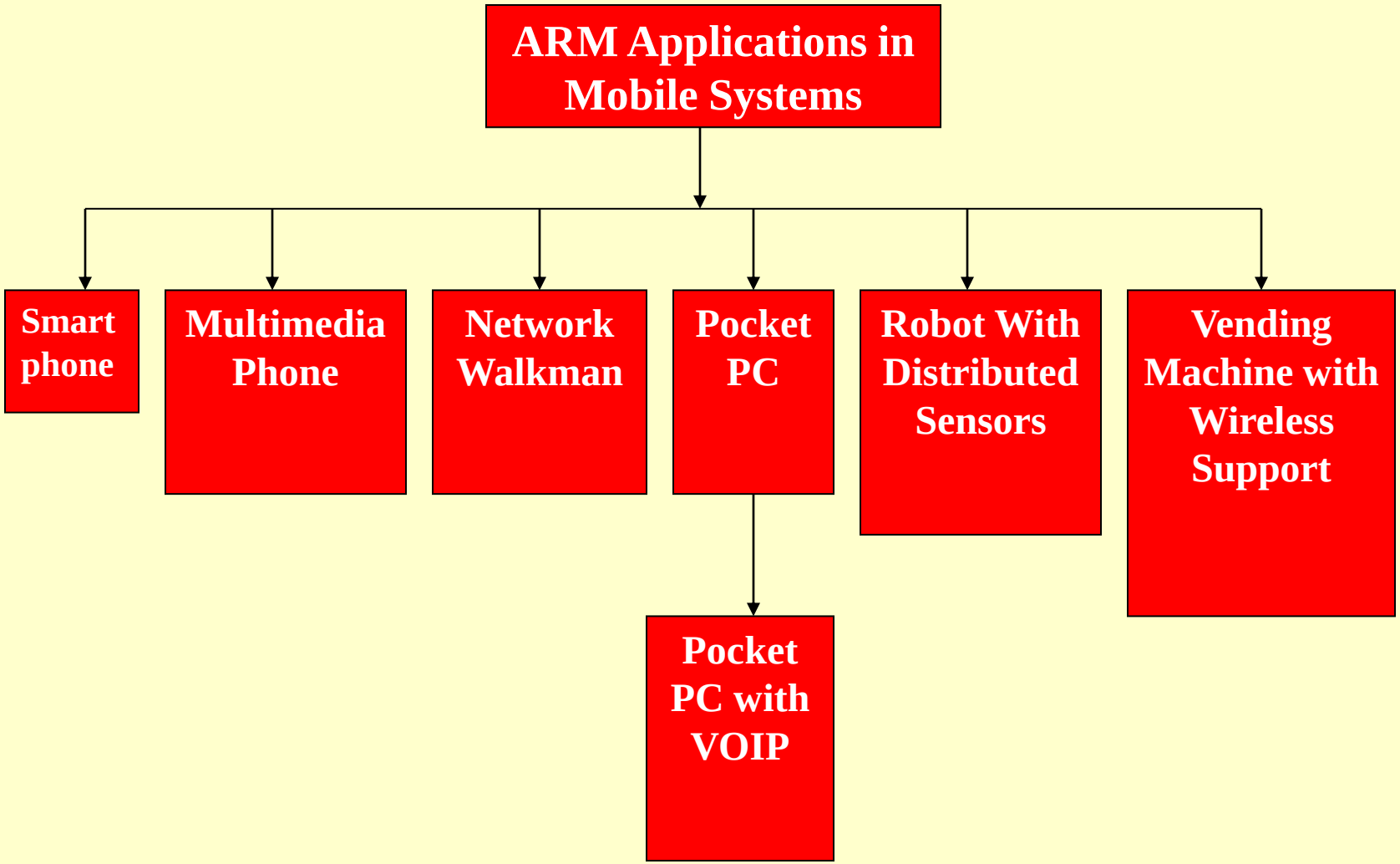


Hardwired Implementation

Examples of Systems needing high-performance precise- computing

- Image processing,
- Video games,
- Robotics,
- Adaptive control and
- Mobile Devices

ARM Applications



Mobile Device CPUs/MCUs

- CPUs ARM-7, ARM-9, ARM11 (More than 50% devices)
- MCUs ST72x, LPC21xx, …
- CPUs PowerPC 750,ColdFire, TigerSHARC

ARM® CPUs options-

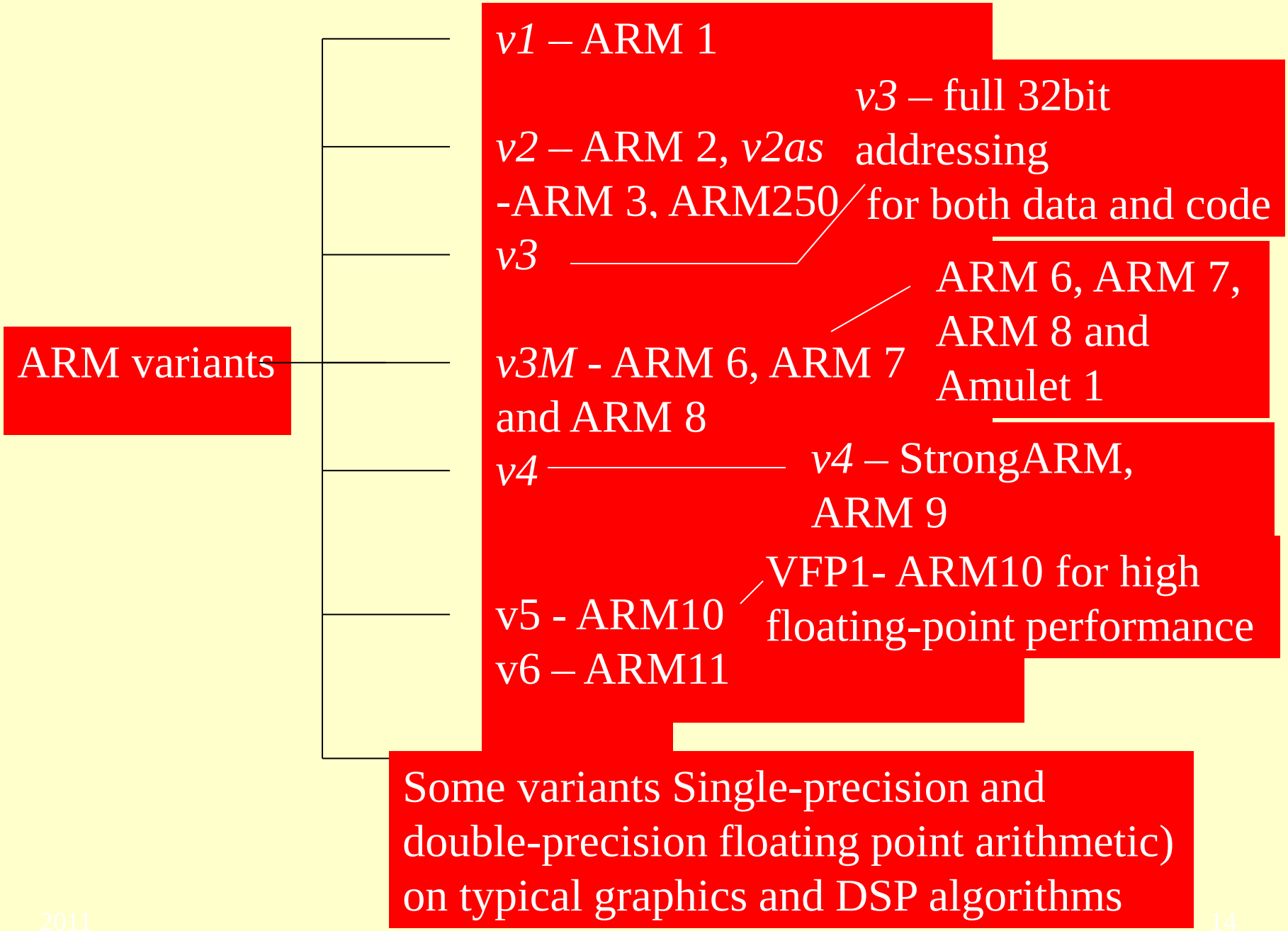
- Extensive range of CPUs with third-party adaptation and application development tools

ARM Many Variant Architectures

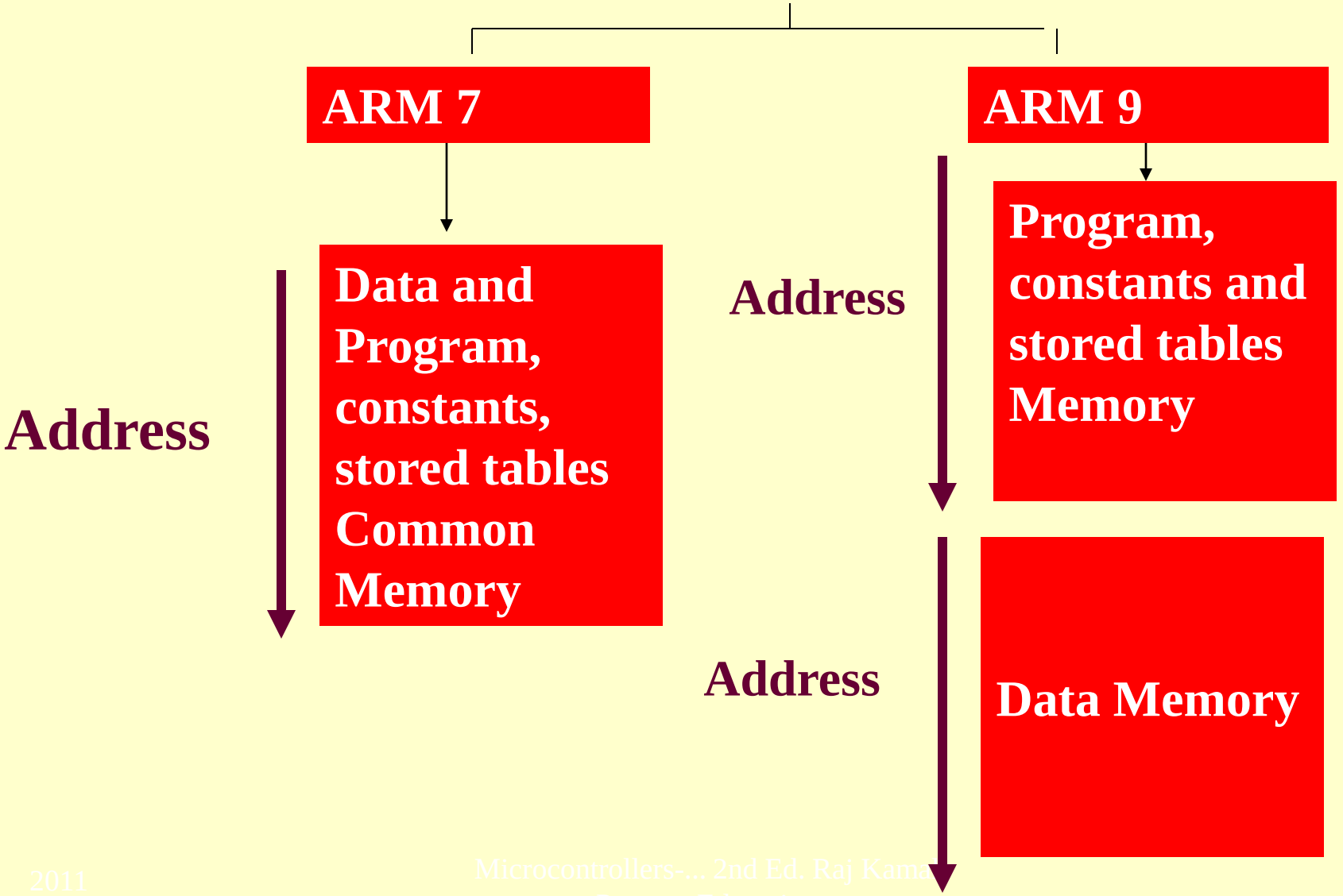
- ARM
- M-variant (v3) Multiply 32× 32 = 64 or 32× 32 +32 = 64
- Thumb (T) variants- Sixteen bit instructions in memory
- DSP varients (v5)
- J- Java Varients (v5)

Versions

- v3— 32-bit address and M-variants
- v4— Half word load and store (ARM9)
- v5— Count leading 0s instructions, ARM 10 VFP-Floating Point Processing- E- Enhanced DSP variants and J- Java execution fast
- v6— Memory management and multiprocessing (ARM11)


ARM variants
v1 – ARM 1
v2 – ARM 2, v2as -ARM 3, ARM250
v3
v3 – full 32bit addressing for both data and code
v3M - ARM 6, ARM 7 and ARM 8
ARM 6, ARM 7, ARM 8 and Amulet 1
v4
v4 – StrongARM, ARM 9
v5 - ARM10
v6 – ARM11
VFP1- ARM10 for high floating-point performance
Some variants Single-precision and double-precision floating point arithmetic) on typical graphics and DSP algorithms

Memory Architecture



ARM® Special **Features**

- Speed-critical control signals pipelining –processing more than one instruction at the fetching, decoding and executing stages.

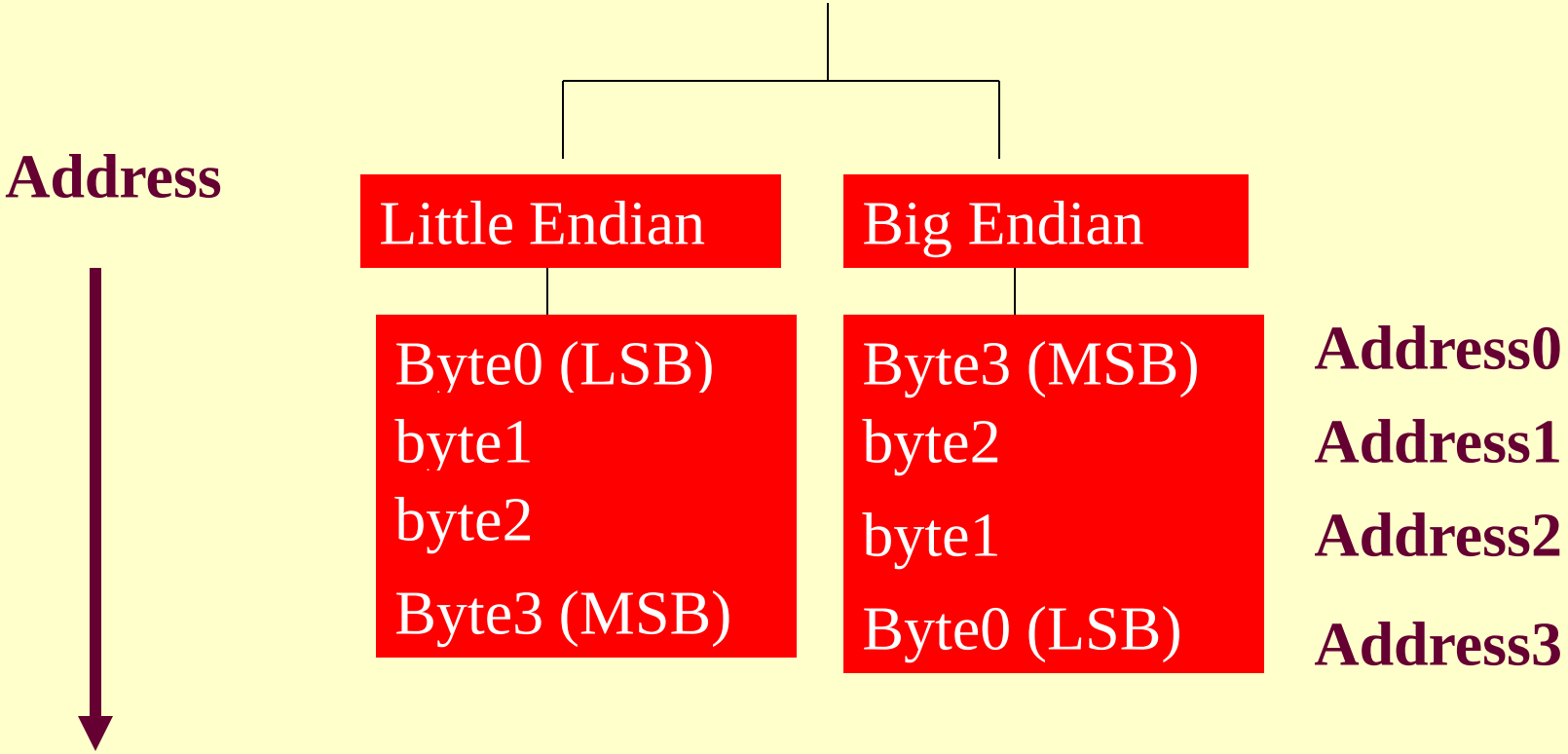
Performance

- ARM 7 and ARM 9 support 300 MIPS (Million Instructions per Second) when die size is 0.13 μm.

Alignment of words

- Processor operation on the words *as per initialization*. A word alignment can then be in *big endian* [least significant byte stored as higher bits (address 3) of a word] or *little endian* [least significant byte stored as lower bits (address 0) of a word].

A 32bit word



Two Initialization options

Static Operation

- Fully static operation- MCU clock can be reduced to 0 and since fully MOSFETs based

Features

- Optimized for fast interrupts and DSP algorithms
- There are two types of requests for interrupts- Fast interrupt request (FIQ) and interrupt request (IRQ). Fast means high priority.
- 4 Gigabytes of linear address space

Features

- 32-bit large set of 16 general-purpose registers with program counter as one of the register (r15) plus CPSR and SPSR -are two other registers.

Features

- System control functions implemented in standard low-power logic
- Cost-effective, compact chip

Summary

We learnt

- ARM family general-purpose 32-bit superscalar processors
- High performance and very low MIPS/watt power consumption
- 32-bit RISC architecture

We learnt

- 32 bit Sixteen Registers plus CPSR and SPSR
- ARM 9 and ARM7 Harvard and Princeton architectures
- Initialized options: little or big endian modes

We learnt

- 32/16/8 bit data types
- Two interrupts - Fast interrupt request (FIQ) and interrupt request (IRQ)

We learnt

- ARM has Many Variants
- T variants give alternate option of high code density with 16-bit instructions

ARM 7 and ARM 9 popularly used

We learnt

ARM applications

- Mobile Devices,
- PocketPC, PDA,
- Control Systems,
- DSP based applications
- Speech and Image processing
- Robotics

End of Lesson 1 on ARM CPUs