Chapter 14

80x96 Family Microcontrollers

Lesson 12

Interrupt Handling System

Interrupt mask bits (primary and secondary level)

- PSW lower byte (SFR at 0x08) saves the mask bits for multiple interrupt source groups and peripheral server enable (PSE) bit to support DMA operations

Interrupt Masks

Primary Mask → **By setting I bit at PSW-Hi**

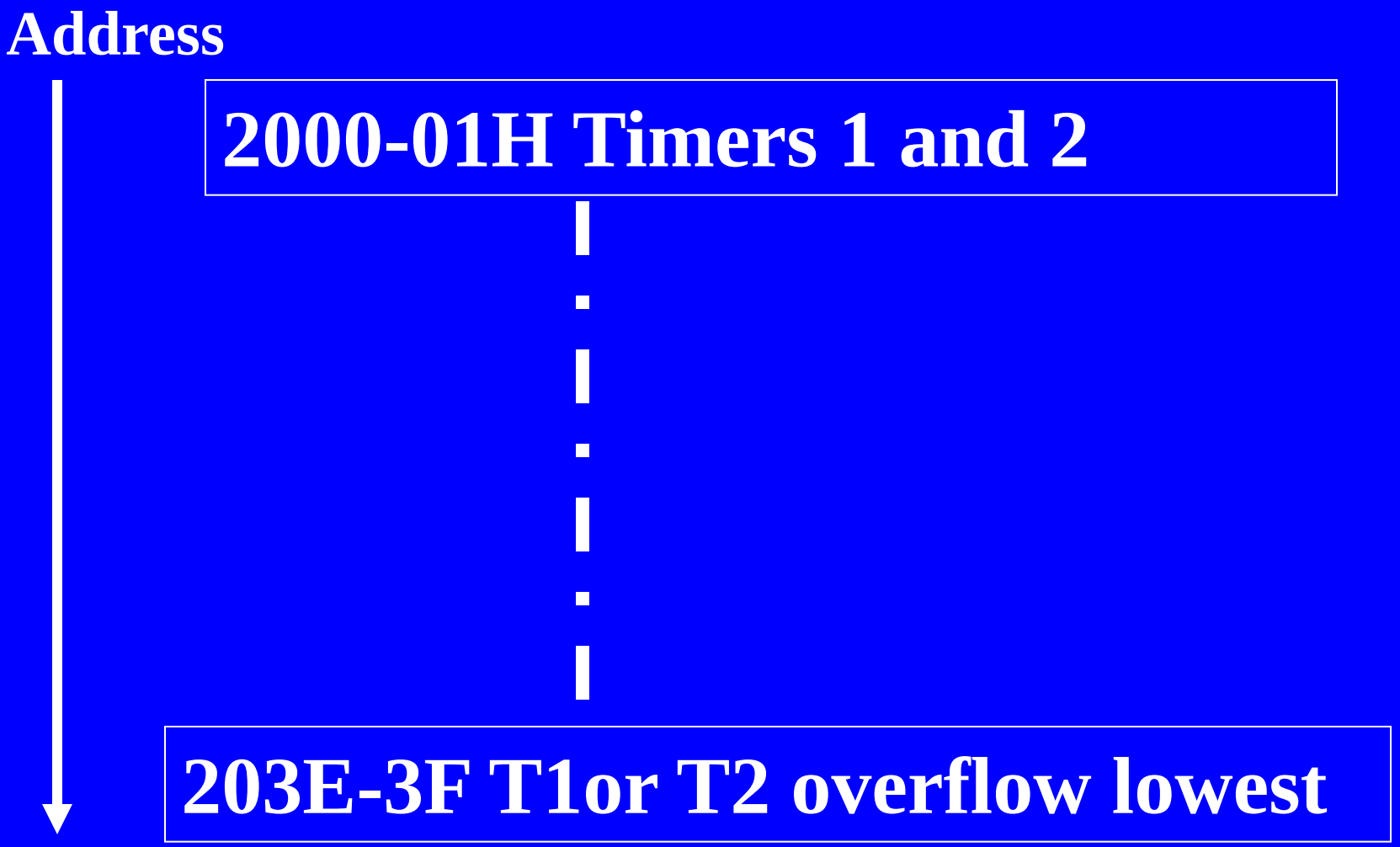
Secondary Masks →

- **INT_Mask PSW-Lo at 08H write**
- **INT_Mask1 at 13H write**

Interrupt vectors

- Between 0x0100H and 0x207F there are P3 and P4 port registers, Interrupt vectors and PTS vectors
- Lower table of interrupt vectors at 2000H to 2013H
- Upper Table at 2030H to 203FH

Interrupt Vectors



Interrupt-mask registers and Interrupt-Pending Registers

- Nine Bytes of SFRs Common in all 4 Windows
- Zero register
- 08H and 13H Two bytes for interrupt-mask registers (one only in 8096)
- 09H, 12H Two bytes for interrupt-pending registers (one only in 8096)
- One byte for window select register
- Two bytes for SPL-SPH.

For Maskable interrupts

Interrupt Identification flag at SP_STAT, IOS1, IOS0

Pending Register → **INT_Pend read at 09H te**

INT_Pend1 at 12H write

Interrupt Pending Identification

interrupt mask register

INT_Mask → When write 08H

INT_Mask1 → When read 13H

interrupt mask register1

Hardware interrupt pins

- EXINT (maskable) [P2.2 external interrupt, EXINT]
- EXINT1 (maskable) [P0.7 EXINT1]
- NMI Interrupt (non-maskable)

Generating interrupt on HSO

- HSO_Command bit b4 [b20]= 1

Generating Timer overflow interrupts

- T1OVIE and T2OVIE interrupt on overflow enable bits to unmask the interrupts on timeouts of timers 1and 2 at IOC1 (Input-Output Control 1 Register).

Software Interrupts

- A Software timer interrupt causes execution of a service routing on successful comparison but no change in an HSO output pin level
- Four software timers are programmable
- Command bits in HSO_CAM at 0x0006 (write)

Flags for interrupts of software timer

- IOS1.0, IOS1.1, ISO.2 and ISO.3, respectively, Software timer 0, software timer 1, software timer 2, and software timer 3 interrupt occurrence flag bits

Seventenn Interrupts

- Interrupt at NMI pin (highest priority) Interrupt at HSI unit
- EXINT1 P0.7 pin Interrupt
- T2 Overflow
- T2 Capture when internal clocking
- HSI FIFO half-full interrupt

Seventenn Interrupts

- Serial Receiver RI set
- Serial Transmitter Empty TI set
- Unimplemented opcode Instruction
- Trap on External Interrupt,

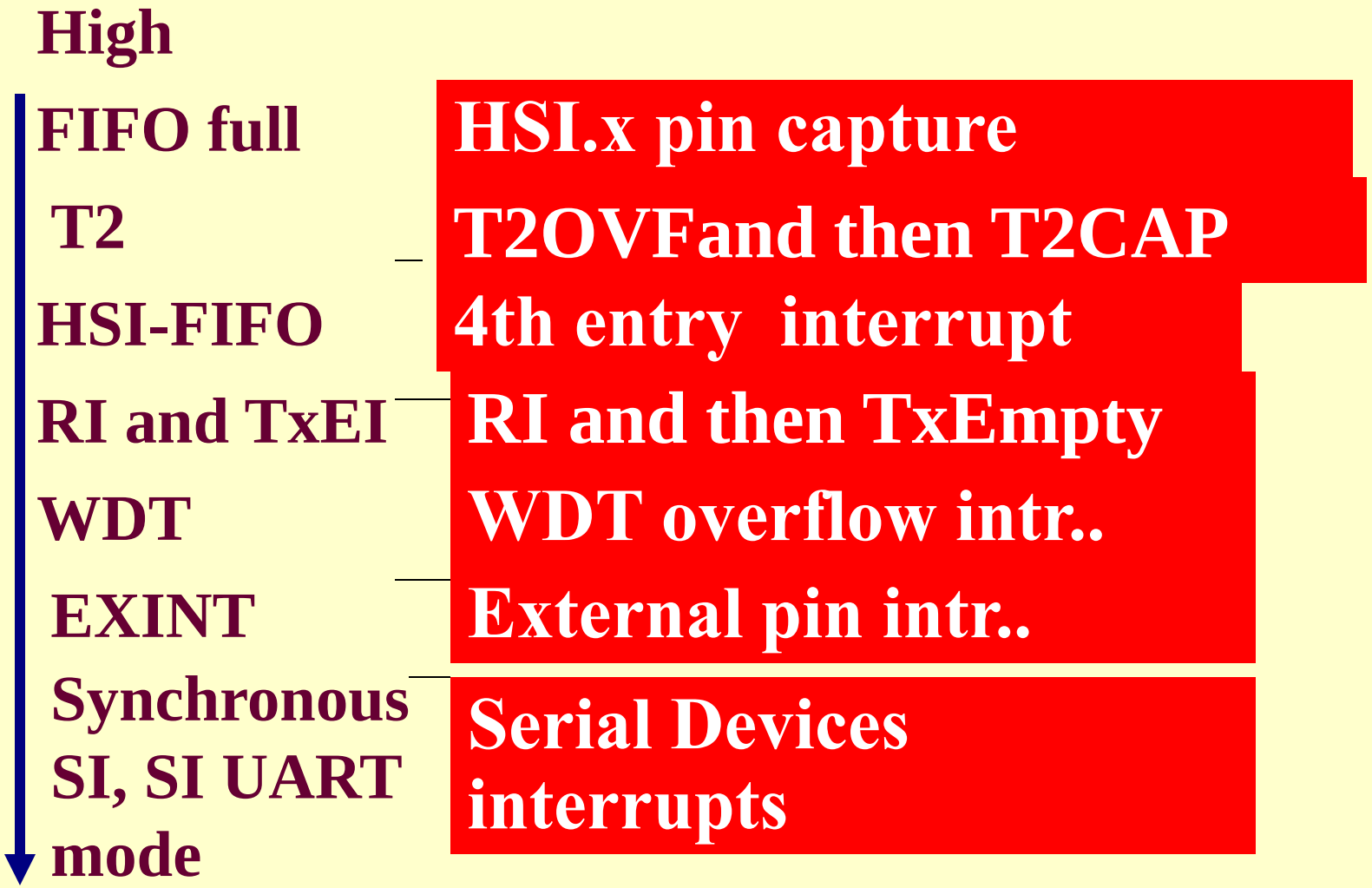
Seventenn Interrupts

- EXINT
- SI interface Interrupts
- Any or both TI (transmitter interrupt) and RI(Receiver Interrupt)
- Software Timers Interrupts,

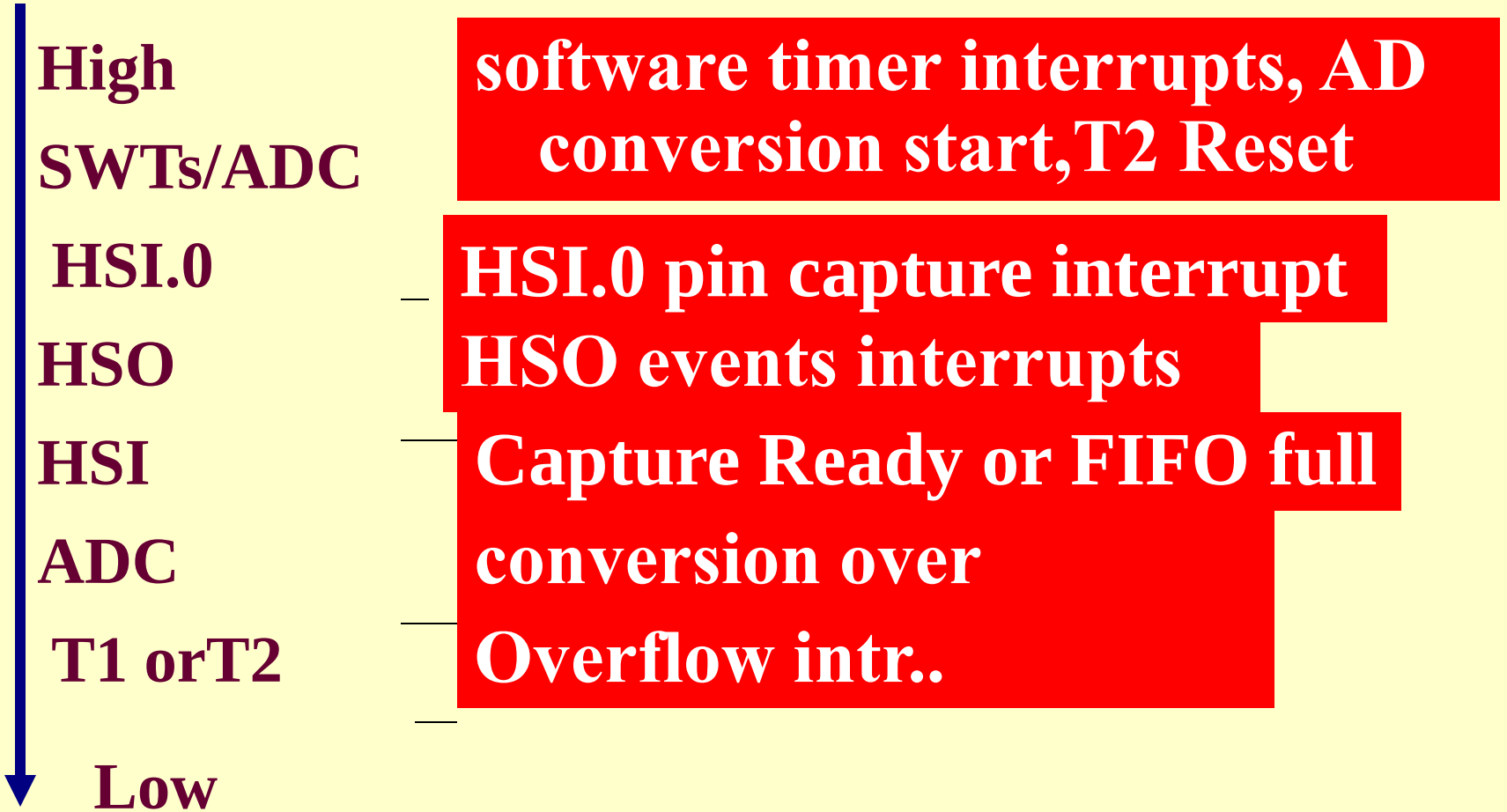
Seventeen Interrupts

- ADCstart at T2 resetHSI pin 0 input instance Interrupt
- HSO Interrupts HSO.0 to HSO.5
- Interrupts from the HSI capture data ready and FIFO full
- A/D conversion over interrupts
- Interrupts from Any or both T1 and T2(lowest priority)

Maskable Interrupts Priority



Maskable Interrupts Priority



Non Maskable Interrupts

- **NMI pin interrupt Highest Priority**

Maskable Interrupts

- Maskable EXINT1 next highest priority
- Maskable T2Overflow next highest
- Maskable T2CAP next highest

Maskable Interrupts

- **HSI-FIFO Half full next highest**
- **RI serial next highest**
- **Tx empty next highest**
- **Unimplemented opcode WDT timeout-next highest**

Maskable Interrupts

- **Software Interrupt**
- **Trap instruction-next to WDT Priority**

Maskable Interrupts

- P2.2 EXINT pin interrupt next highest
- Any TI or RI SI interrupt next highest
- 4 SWTs interrupts
- ADC start
- T2 reset next highest

Maskable Interrupts

- HSI.0 pin time-capture interrupt next highest priority
- HSO.0-HSO.5 interrupt next highest
- HSI capture data ready
- FIFO full interrupt next highest

Maskable Interrupts

- AD conversion over next priority
- Either T1 or T2 overflow lowest priority

Steps in Interrupt ISR Start and Return

Priority	→ Default Assignments
Push	→ PCH, PCH on to stack
Pre emption	→ Yes in between preemption by higher priority interrupt if not defined as masked
Pop	→ PCH, PCH from stack

Summary

We learnt

- Interrupt Handling System
- Interrupt Vectors
- Interrupt masks
- Hardware interrupt pins
- Interrupt Priorities

End of Lesson 12 on

Interrupt Handling System