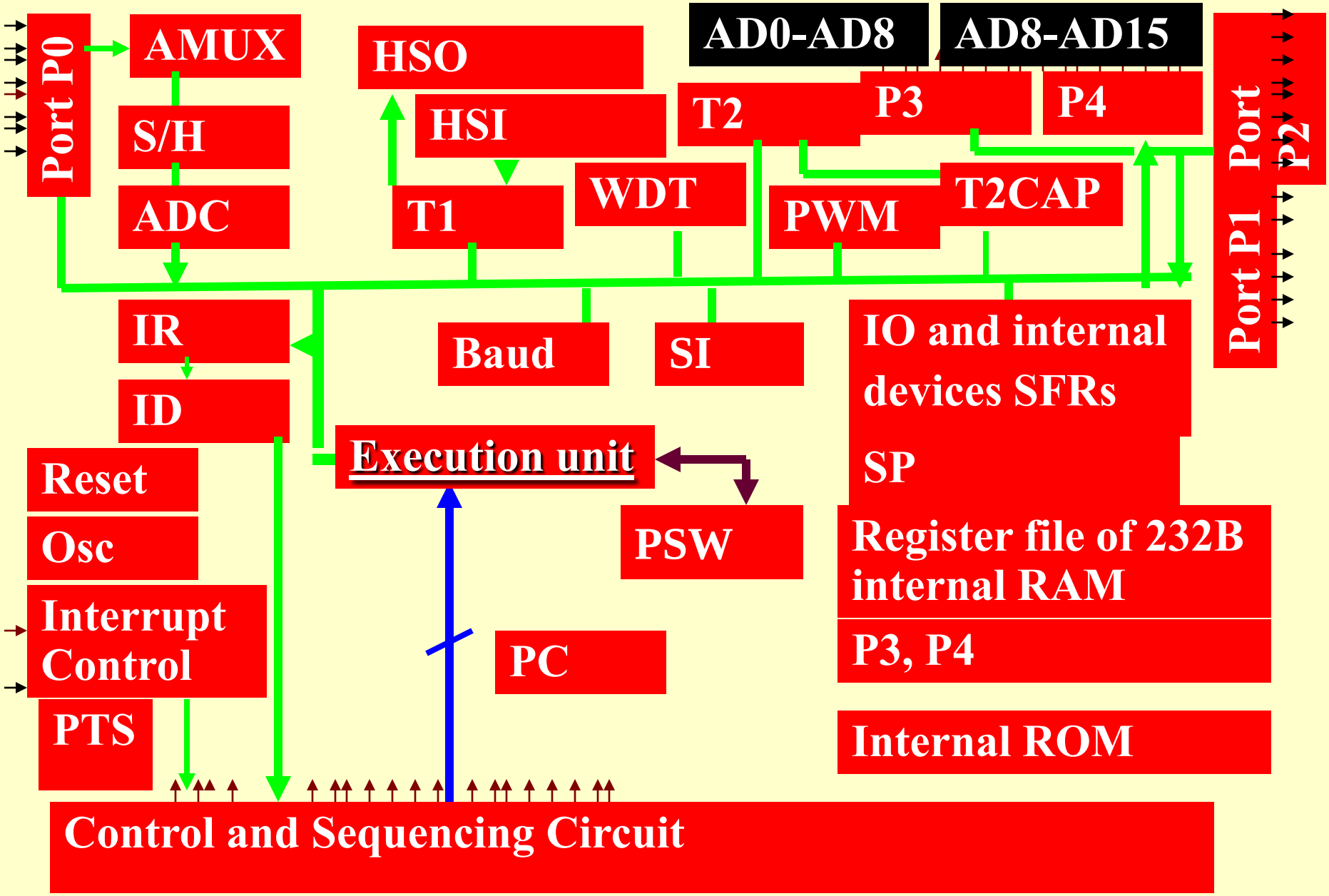
Chapter 14

80x96 Family Microcontrollers

Lesson 08 Part a

80x96
Timers T1 and T2


Port P0
AMUX
S/H
ADC
HSO
HSI
T1
WDT
AD0-AD8
AD8-AD15
T2
P3
P4
PWM
T2CAP
Port P2
Port P1
IR
ID
Baud
SI
IO and internal devices SFRs
SP
Execution unit
PSW
Reset
Osc
Interrupt Control
PTS
PC
Register file of 232B internal RAM
P3, P4
Internal ROM
Control and Sequencing Circuit

16-bit Free running counter T1

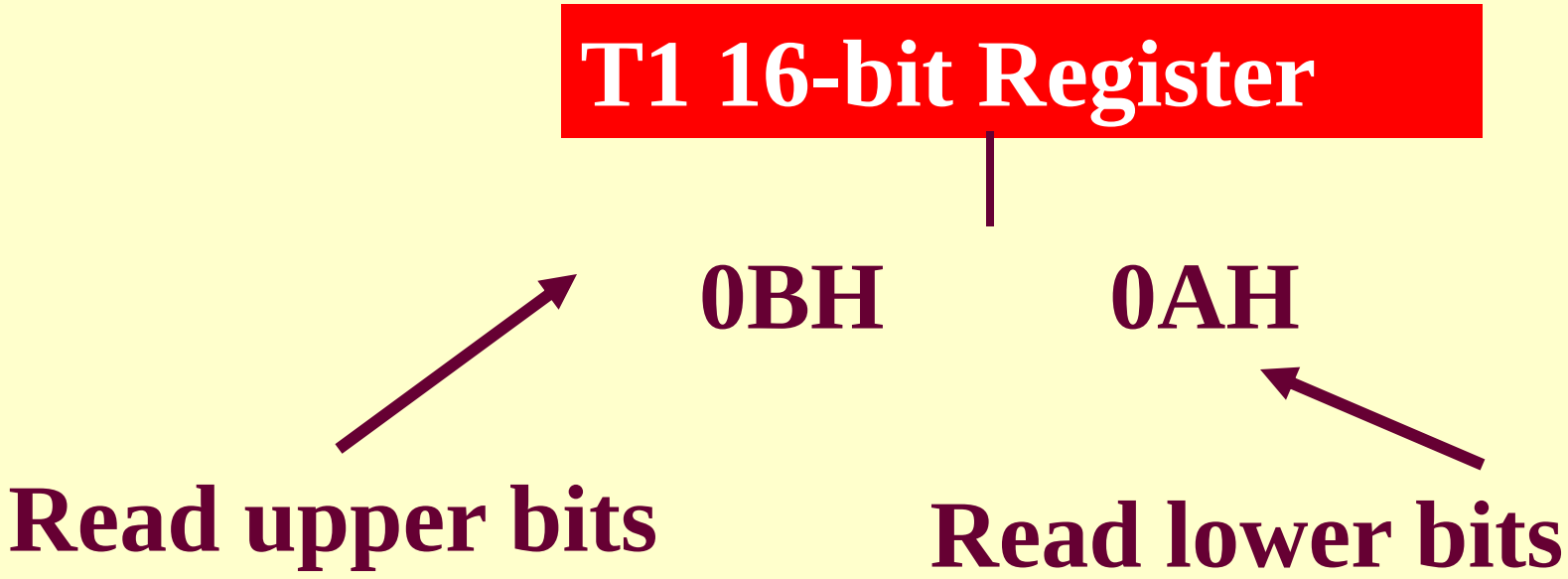
- Gets inputs from clock (0.5 MHz) for 12 MHz XTAL
- No stop, No write for load and no reset
- Reads on instruction for store or add or other executes

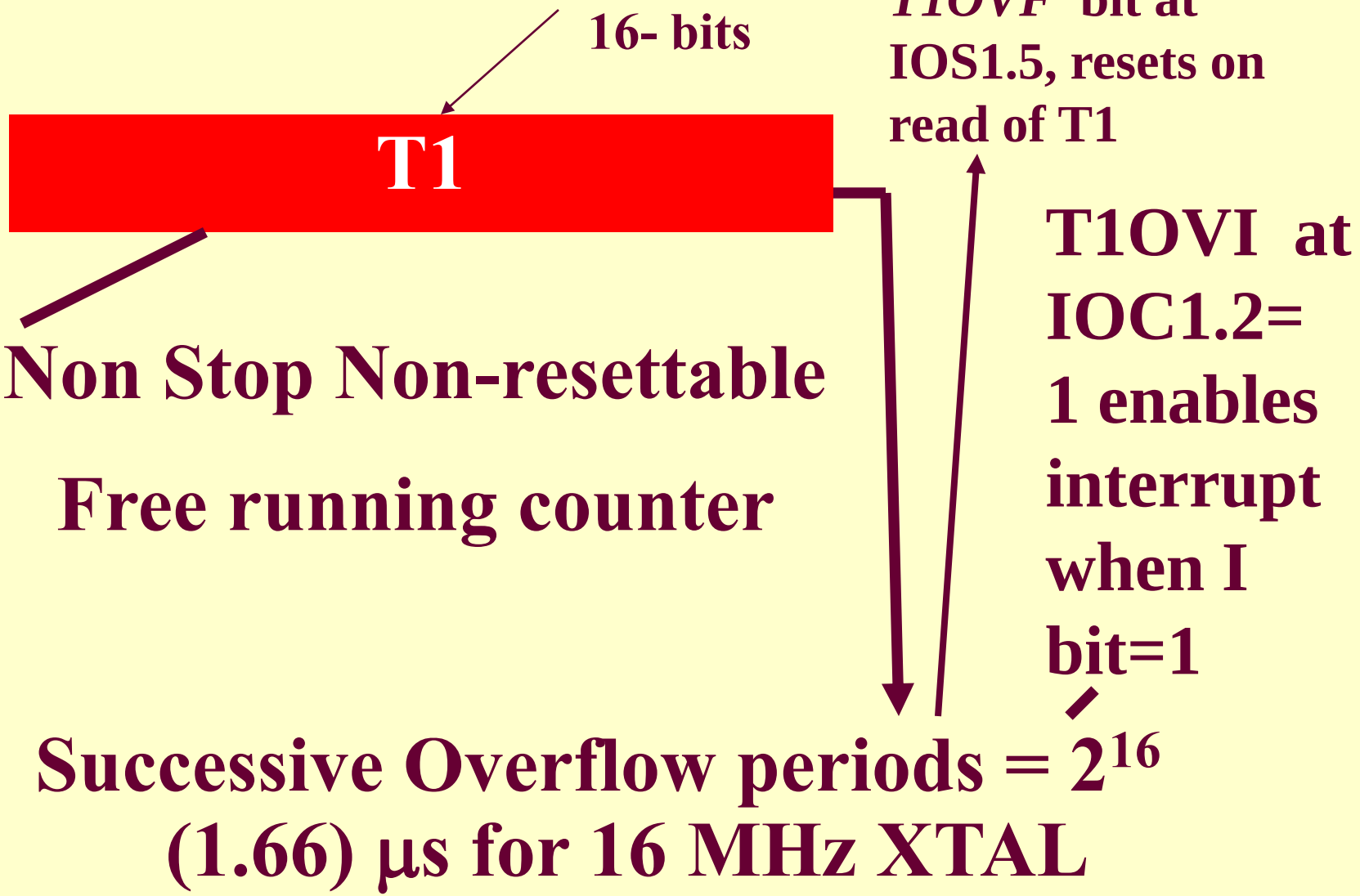
16-bit Free running counter T1

Inputs period = 2 μs for 12 MHz XTAL

= 1.66 μs for 16 MHz XTAL

Free Running Timer-Counter T1 Register




16- bits
T1
T1OVF bit at IOS1.5, resets on read of T1
T1OVI at IOC1.2= 1 enables interrupt when I bit=1
Non Stop Non-resettable
Free running counter
Successive Overflow periods = 2^{16}
(1.66) μs for 16 MHz XTAL

16-bit Event counter T2

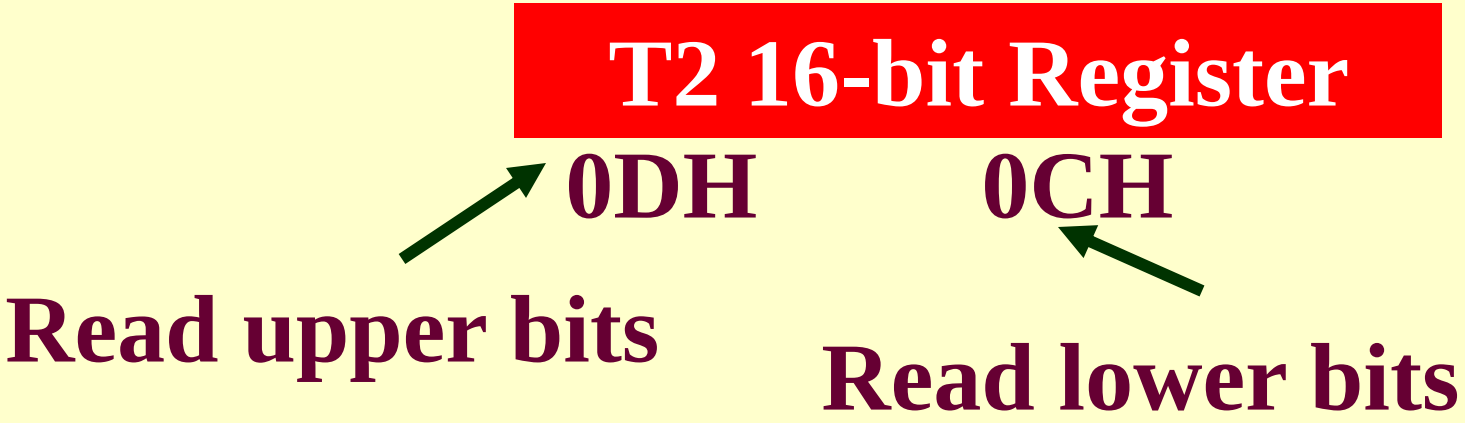
- Event counter T2 gets clock inputs from T2CLK pin (P2.4) or HSI.1
- IOC0.1 → 1 force reset
- Reset can also be forced by HSI.0 input capture when IOC0.0 = 1
- Resets by input T2RST pin (P2.3) when IOC0.3 → 1

T2

- T2 Increments by HSI.1 pin input when IOC0.2 = 1,
- Increments by +ve edge HSI.1 pin input when IOC0.7 = 1 (provided enabled by IOC0.2), else by T2CLK when IOC0.7 = 0.
- WhenIOC0.5 = 1, T2 inputs programmable +ve edge at HSI.0, +ve edge at T2CLK pin when = 0.

Timer-Count T2 Register

+ve edge or -ve edge input programmable



Summary

We learnt

- T1 Free running counter
- T1 Inputs period = 2 μs for 12 MHz XTAL
- = 1.66 μs for 16 MHz XTAL

We learnt

- T2 Input Event Counter
- T2 Increments by +ve edge HSI.1 pin input when IOC0.7 = 1 (provided enabled by IOC0.2), else by T2CLK when IOC0.7 = 0.
- WhenIOC0.5 = 1, T2 inputs

- T1 or T2 when overflows then if not masked interrupt occurs

End of Lesson 8 Part a on Timers – T1 and T2