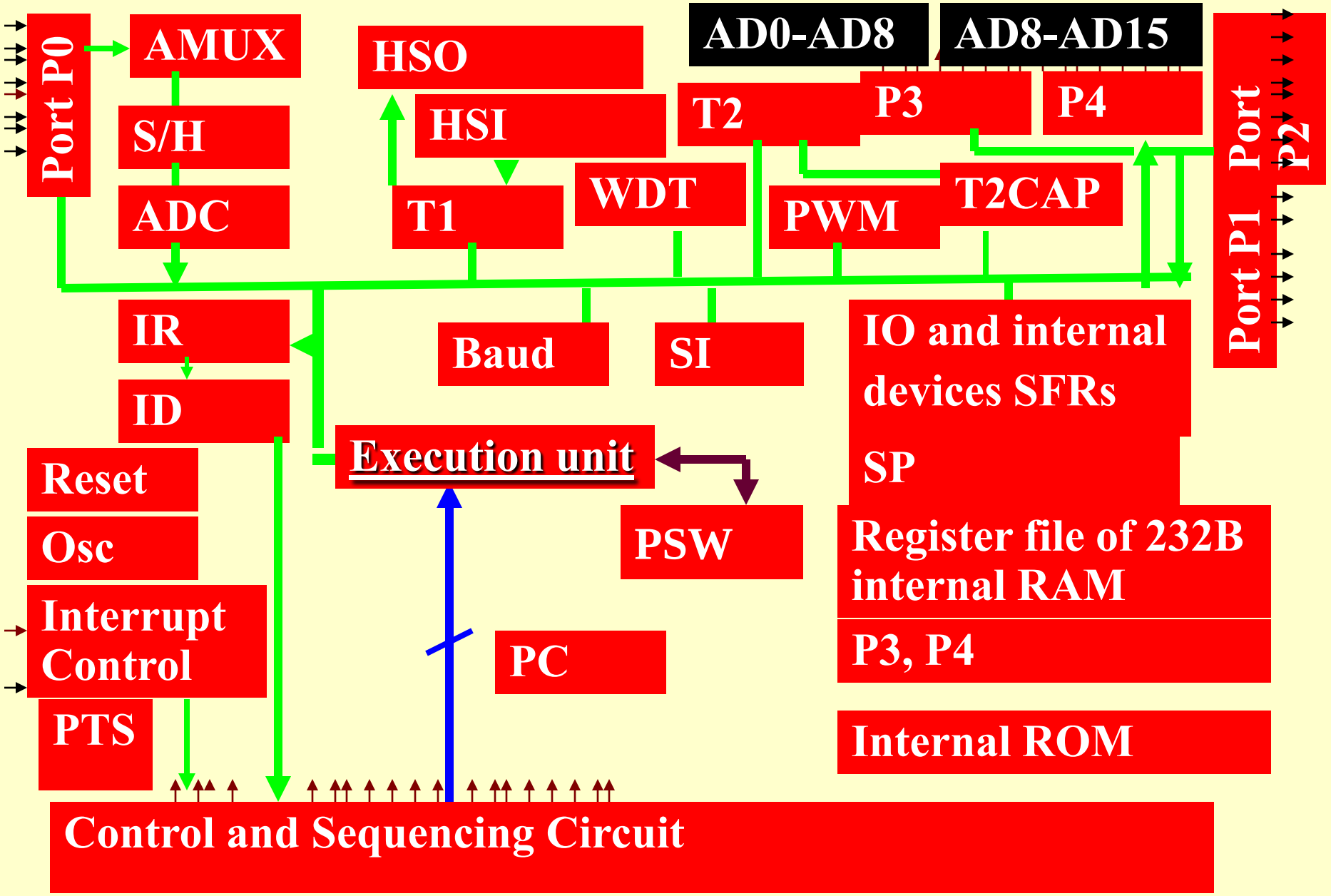
Chapter 14

80x96 Family Microcontrollers


Port P0
AMUX
S/H
ADC
HSO
HSI
T1
WDT
AD0-AD8
AD8-AD15
T2
P3
P4
PWM
T2CAP
Port P2
Port P1
IR
ID
Baud
SI
IO and internal devices SFRs
SP
Execution unit
PSW
Reset
Osc
Interrupt Control
PTS
PC
Register file of 232B internal RAM
P3, P4
Internal ROM
Control and Sequencing Circuit

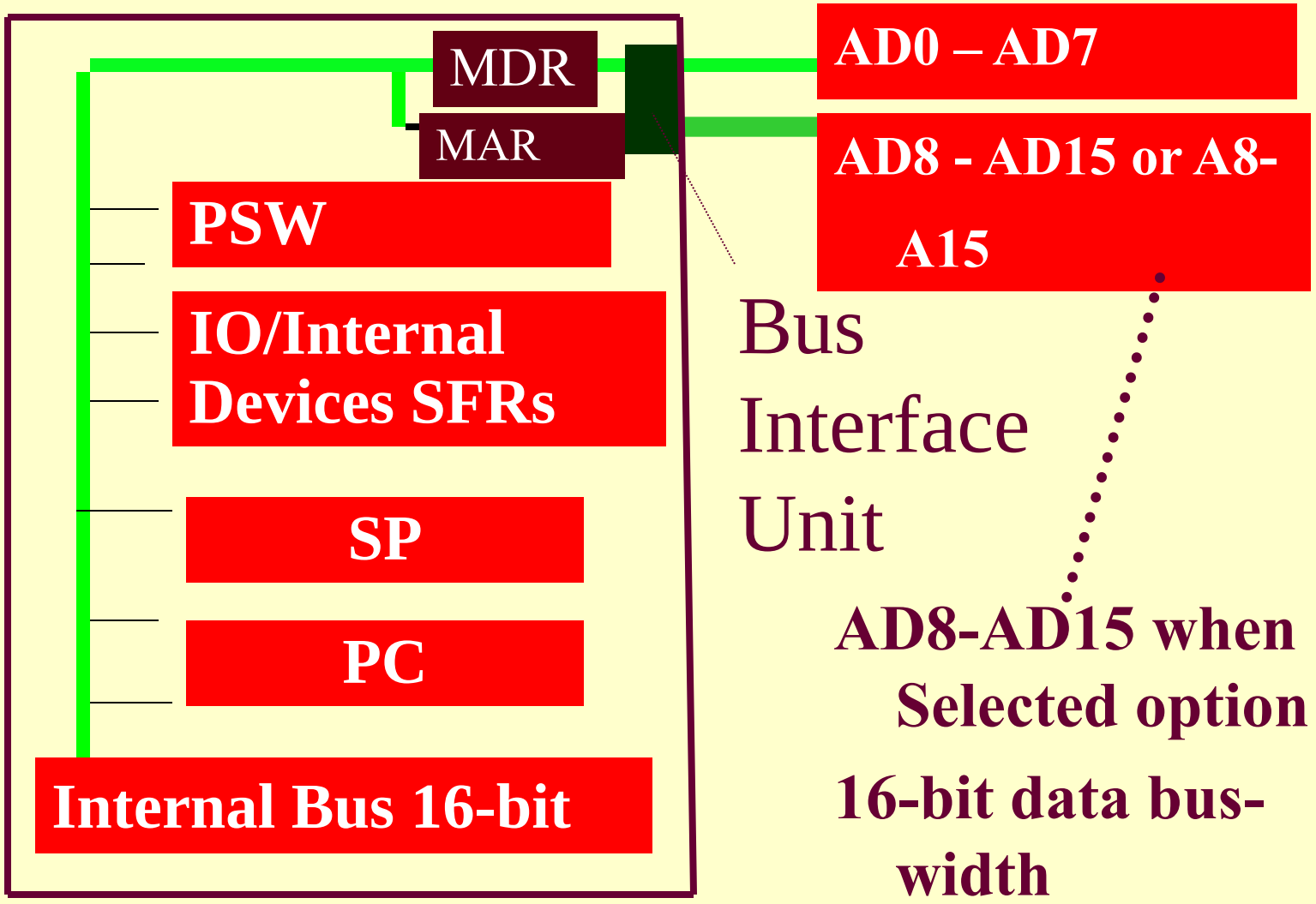
Lesson 1

80x96 Architecture overview

CPU Performance

- 16-bit internal bus and 16 bit address
- 16/8 bits (selectable options) external data bus
- Result in higher processing rate than an 8-bit CPU
- 12/16 MHz XTAL- High clock rate

Internal and External Buses

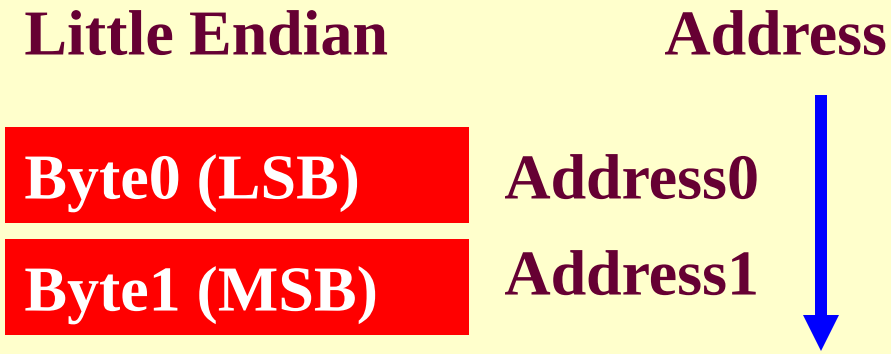


CPU Registers

- 16-bit Program Counter PC
- 16- bit PSW (Processor Status Word)
- 16-bit Stack Pointer SP (Also a memory address)
- A 16-bit Register lower byte saves in memory at even and upper byte at odd address) [Little Endian Word alignment]

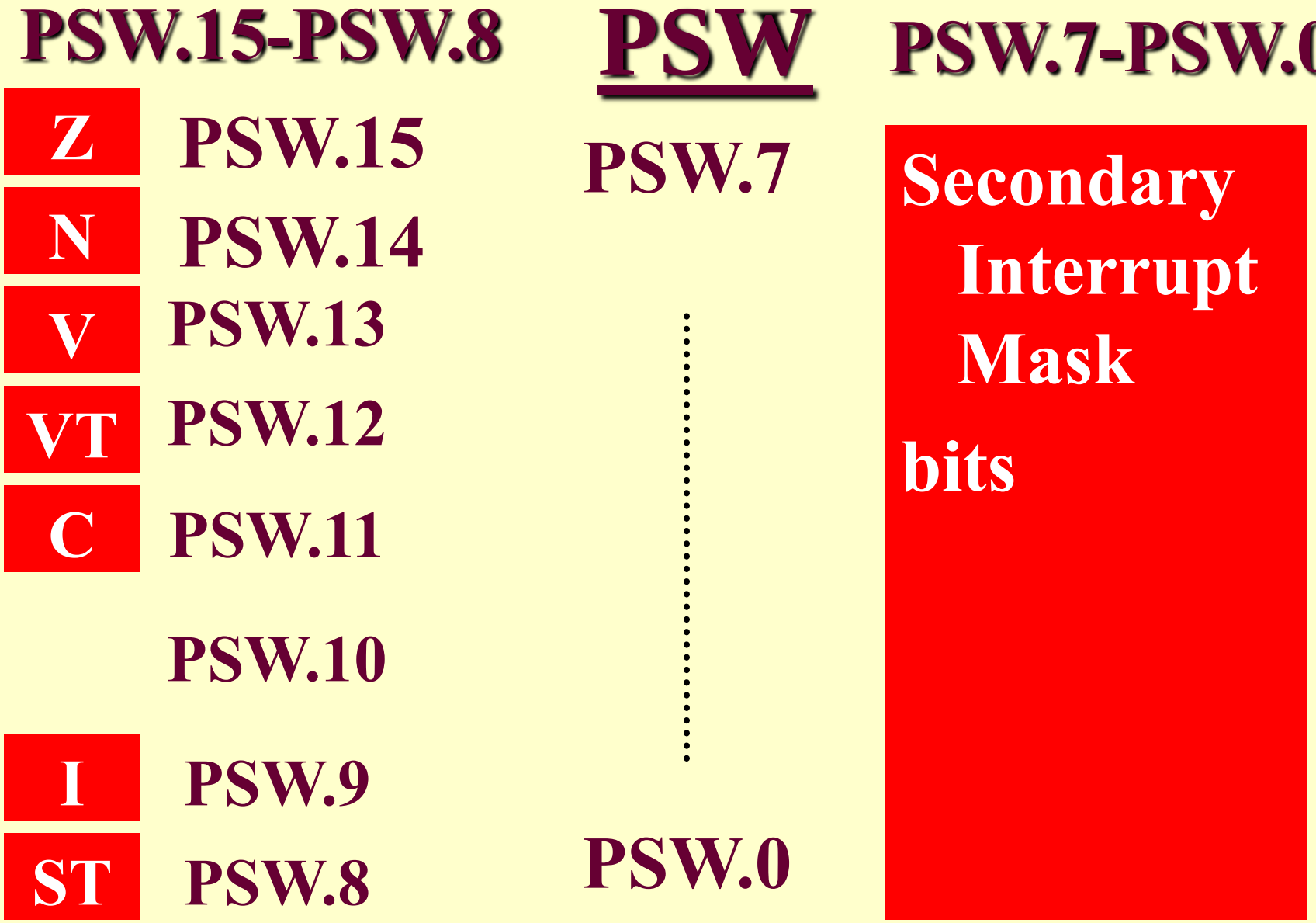
16-bit word alignment

A 16bit word in memory



PSW

Z	Zero flag
N	Negative Flag
V	Overflow flag
VT	Overflow trap flag
C	Carry flag
I	Primary interrupt enable bit
ST	Sticky bit flag


PSW.15-PSW.8
PSW
PSW.7-PSW.0
Z
PSW.15
N
PSW.14
V
PSW.13
VT
PSW.12
C
PSW.11
PSW.10
I
PSW.9
ST
PSW.8
PSW.7
PSW.0
Secondary Interrupt Mask bits

CPU Instructions

- 16 as well as 8-bit data type Instructions
- Processor operation of 16-bit data type is as per word alignment at memory in *little endian* [least significant byte stored as lower bits (address 0) of a word]

MCU Architecture overview

- 80x96 common 16-bit internal bus for the 16-bit addressing and 16/8-bit data
- Princeton architecture bus
- Bus interface for 16-bit/8-bit data and instructions

16-bit SP Address – 0018H

SPL

Byte Address – 0018H

SPH

Byte Address – 0019H

SP Increases before push, decreases after pop

Interrupts

- Two Maskable Interrupt requests EXINT1 at P0.7 Interrupt and EXINT and one unmaskable (NMI) interrupt

Program Counter

- Program Counter (PC) initializes at 2080H-2081H on Reset

Timers

- Timer T1 as a free running counter
- An additional timer T2 with reset external clocking inputs

Watchdog Timer

- A watchdog timer

Serial Interface

- Serial Interface SI-option UART full duplex or half duplex serial synchronous bits with separate clock bits

High Speed Output on compares

- HSO High speed outputs

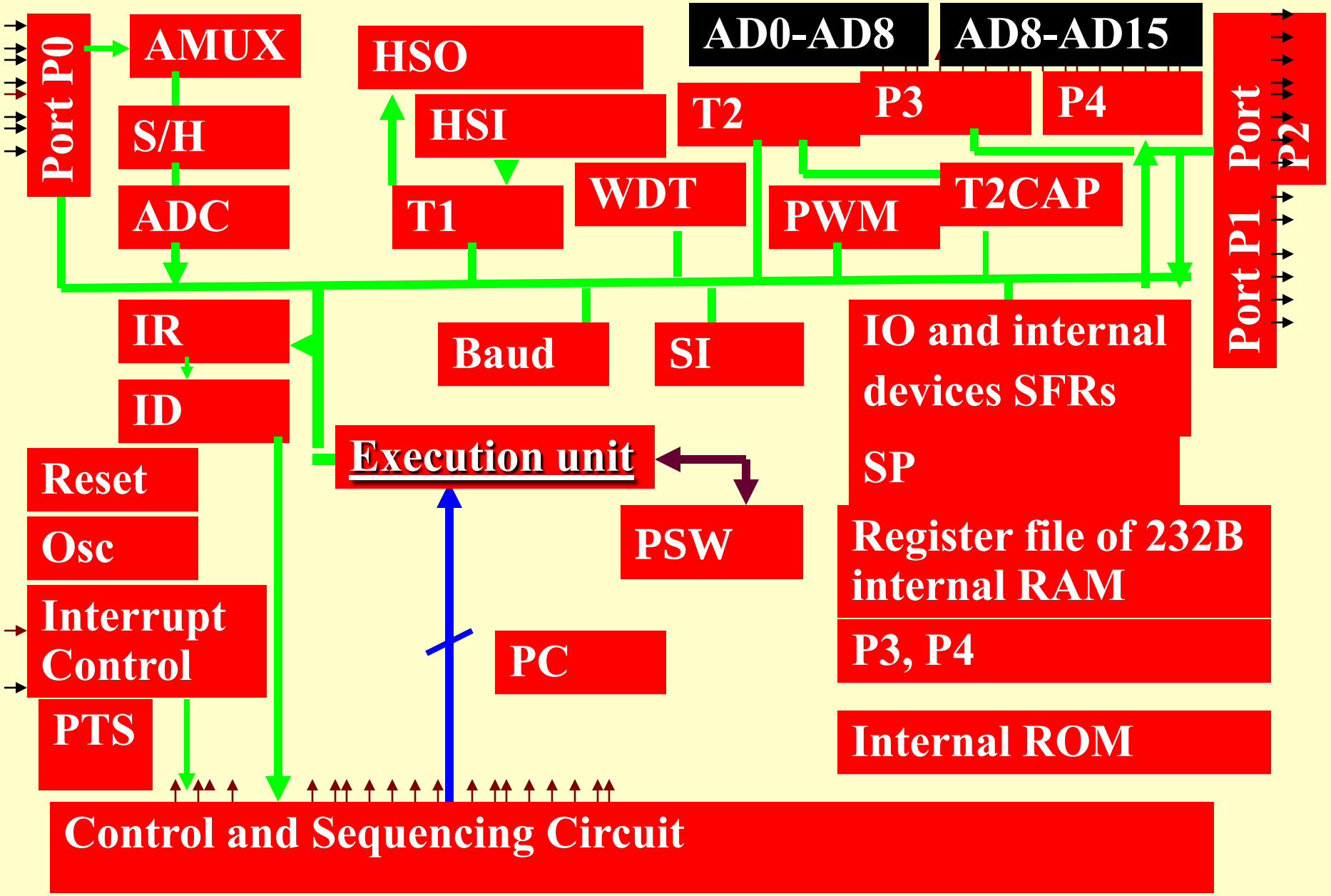
High Speed Input Captures

- HSI High Speed inputs

ADC

- Multi channel ADC

80x96 Architecture view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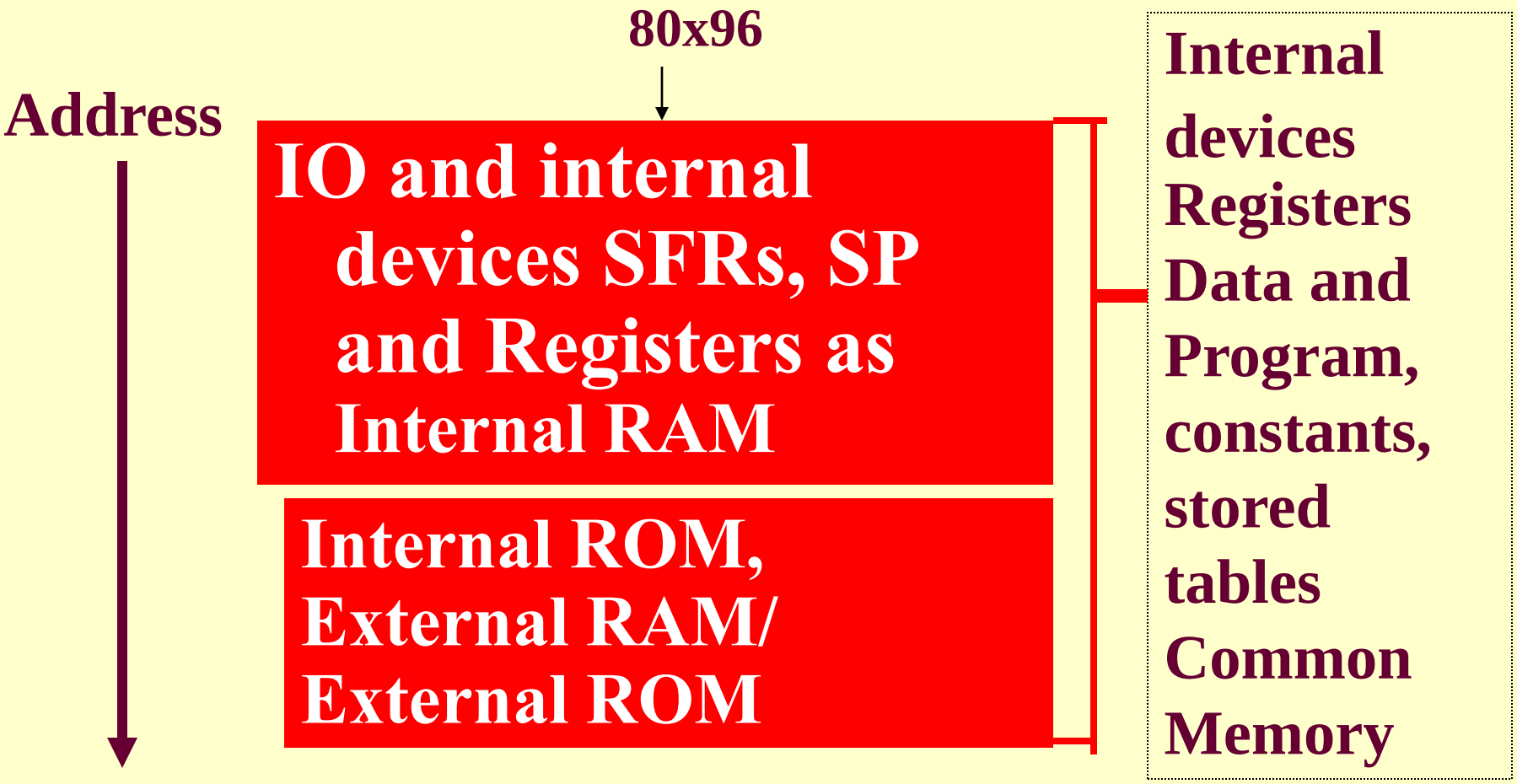
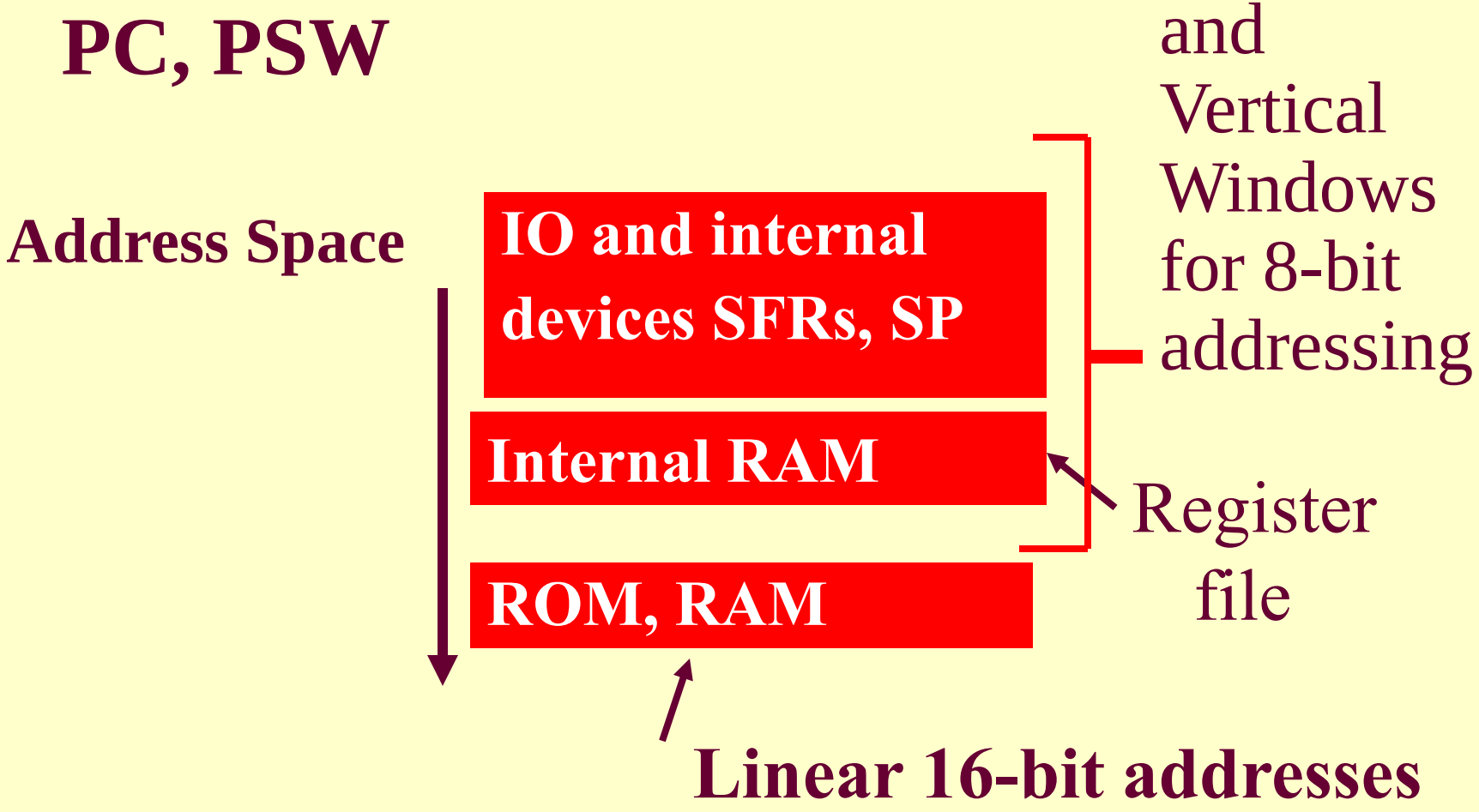
64 kB address space with H and V windows
Memory Architecture



80x96 Family Programming Model



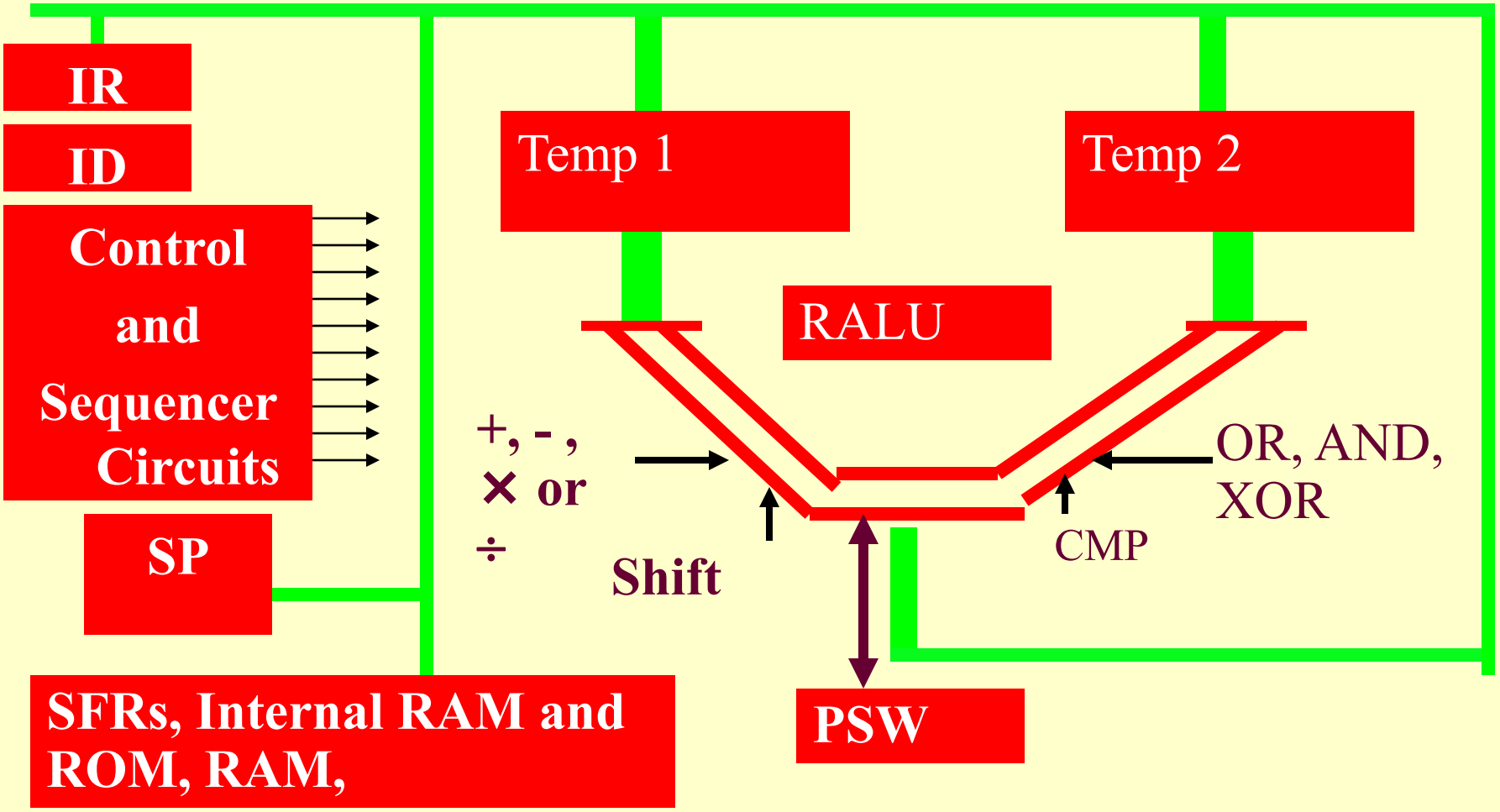
Horizontal and Vertical Windows for 8-bit addressing

- H and V windows Page 0 addressable by 8-bits for 0000H-00FFH Internal RAM can be used as registers

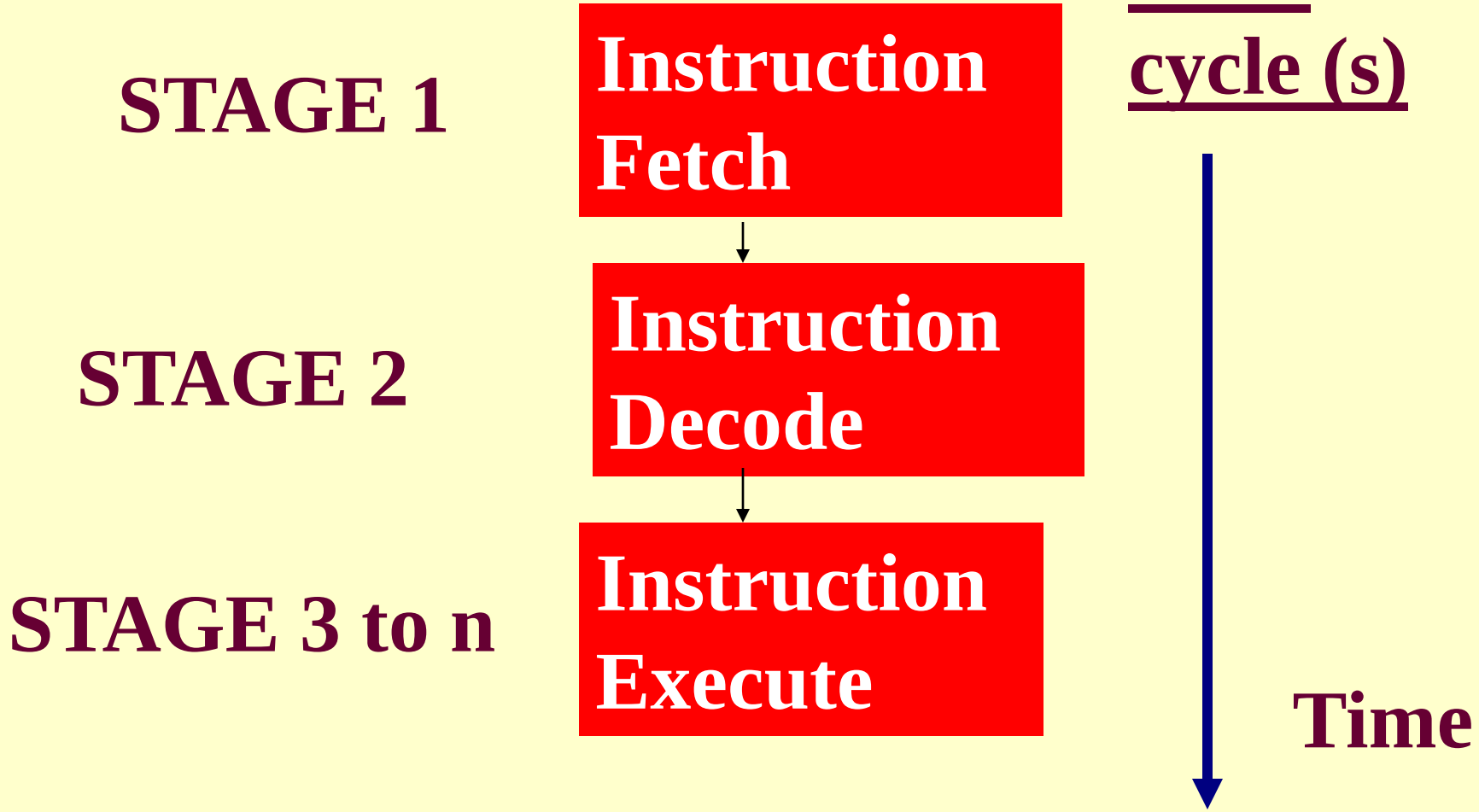
RALU

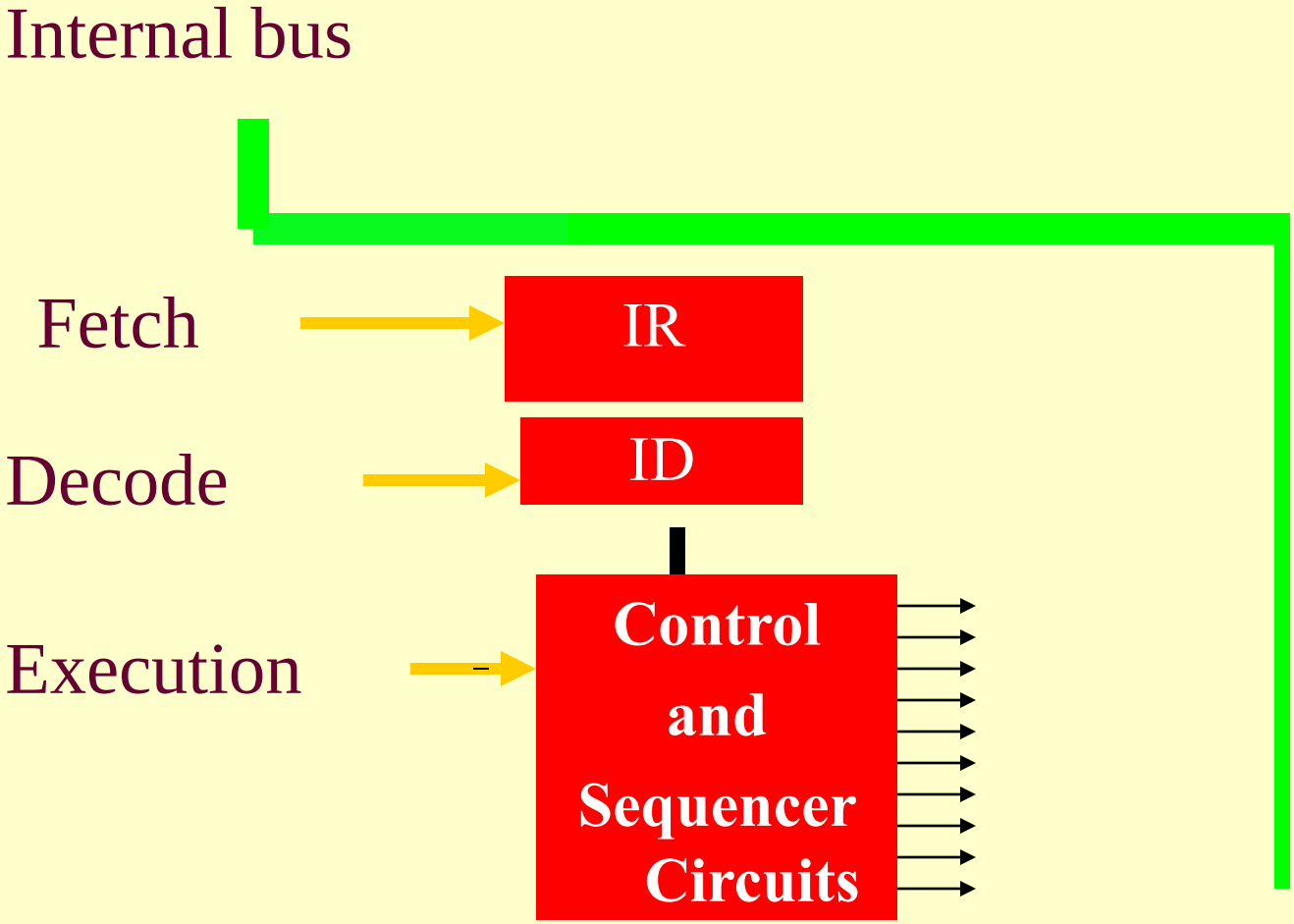
- *multiplier* and *divide*

Execution Unit



Instruction Execution





Control memory micro codes based-Implementation

Ports

- Expanded Mode used for interfacing External Memory and Ports P0 to P4

Summary

We learnt

- 80x96 family 16-bit processor
- PC, SP, PSW
- Princeton architecture
- 16/8 bit data types
- Little endian 16-bit word alignment
- Interrupts – Maskable Interrupt requests (EXINT, EXINT1) and unmaskable (NMI)
- PC = 2080H at reset

We learnt

- IO/Devices Control and Status SFRs, SP, Internal RAM – H and V windows 8-bit addressing
- Internal ROM
- RAM/ROM

We learnt

Internal Devices

- T1free running counter and T2
- SI
- HSOs
- HSIs
- Multi channel ADC

End of Lesson 1 on 80x96 Architecture overview