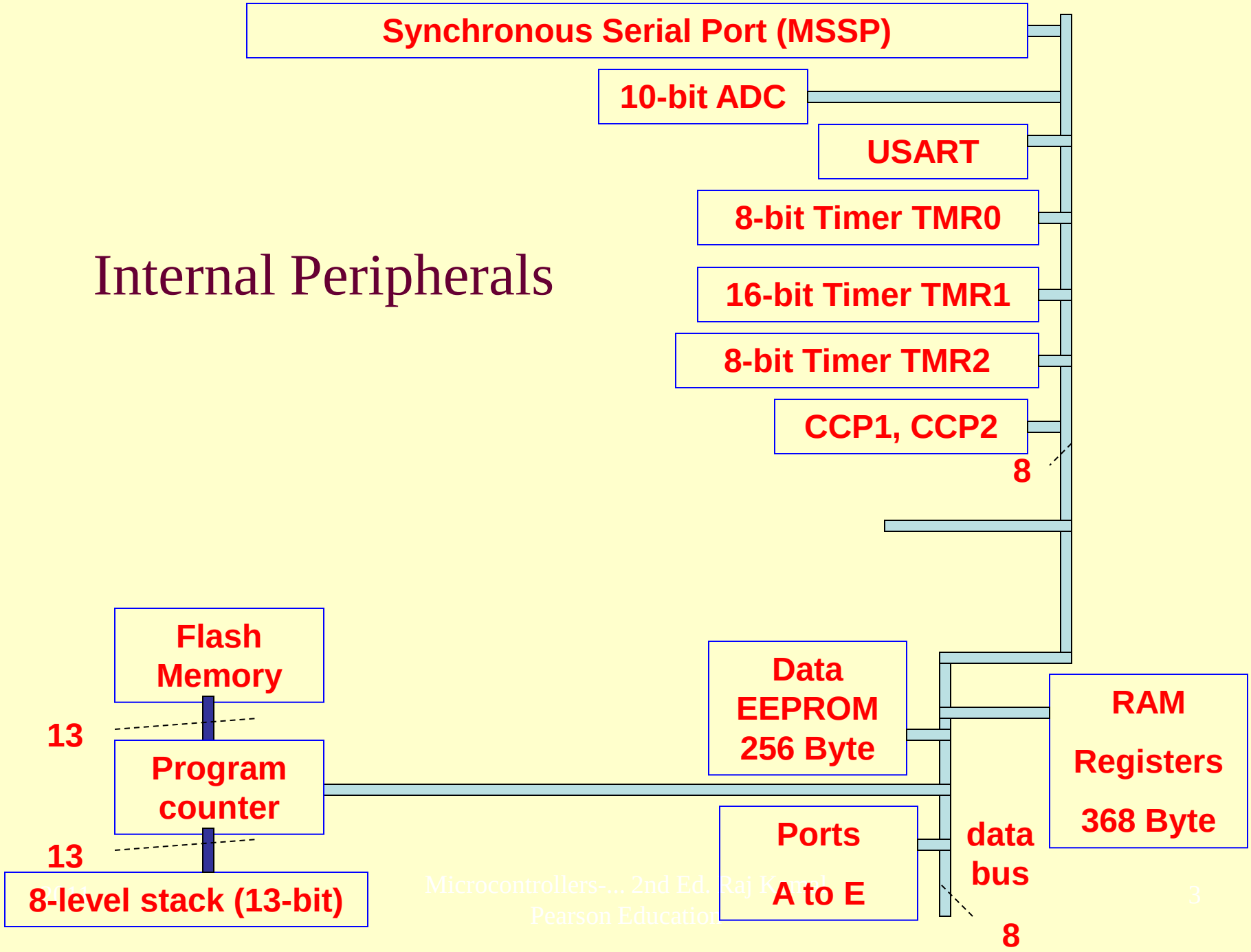
Chapter 13

PIC Family Microcontroller

Lesson 12

Pulse Width Modulation Outputs 1 and 2 using CCP1 and CCP2

Internal Peripherals



Pulse width Modulated PWM output Pulse period and Output period

- PWM output has a time-base period (pulse-period) and PWM pulse frequency. Pulse period = 1/ pulse-frequency.
- Assume that time period for output 1 = 4 ms and output 0 = 16 ms, then pulse period = (4 ms + 16 ms) = 20 ms. Pulse frequency = 1000/20 = 50 pulse per second.
- Duty cycle = time period for 1/Total Period = 4 ms/16 ms = ¼ = 25%.

Pulse width Modulated PWM output

- The pulses of period for output 1 proportional to the bits in a register called pwm_register.
- pwm_register–a register used for generating the PWM output pulse periods.
- It means 16-bit register will have value ¼ of 2^{16}, if duty cycle = ¼ = 25%.
- PWM output on integration generates an analog output, linearly related to bits in a register pwm_register

Pulse width Modulated PWM output

- If 10-bit pwm_register has bits = 00 0100 0000 0000, it means 1/16 of maximum value, then PWM output duty cycle = (100/16)% and PWM output on integration generates an analog output, 1/16 times the maximum analog output when duty cycle = 100%.

CCP1 controlled PWM1 output duty cycle

- PWM1 output at RC2/CCP1 pin
- PWM resolution 10 bit [Duty cycle can be from $1/2^{10} = 1/1024$ to 1 = (1/1024)% to 100%.
- One of the modes for CCP1– PWM peripheral device 1
- CCPR1L is used to define duty cycle 8-bits.
- 2 bits written at CCP1CON bits b5-b4

CCP1 controlled PWM1 output duty cycle

- Duty Cycle PWM1 = 10 bit value in CCP1CON and CCP1L /2^{10}.

CCP2 controlled PWM2 output duty cycle

- A PWM output enables at RC1/CCP2 pin
- PWM resolution 10 bit
- One of the modes for CCP2–PWM peripheral device 2)
- CCPR2L is used to define duty cycle 8-bits.
- 2-bits written at CCP2CON b5-b4 to write remaining bits for duty cycle

CCP2 controlled PWM2 output duty cycle

- Duty Cycle PWM2 = 10 bit value in CCP2CON and CCP2L /2^{10}.

CCP1 register use in PWM mode

- 8-bits out of 10-bits for the PWM mode of CCP1 at CCPR1L and that copies to CCPR1H on reset
- CCPR1L is written and read using address 0x15 (bank 0 SFR)
- CCPR1H is read only in PWM mode
- The address 0x16 (bank 0 SFR)

CCP1 control register

- CCP1 control register CCP1CON, written or read using 0x17H

CCP2 register use in PWM mode

- 8-bits out of 10-bits for the PWM mode of CCP2 are at CCPR2L and that copies to CCPR2H on reset
- CCPR2L written and read using address 0x1B (bank 0 SFR)
- CCPR2H is read only in PWM mode
- The address 0x1C (bank 0 SFR)

CCP2 control register CCP2CON

- CCP2 control register CCP2CON, written or read using 0x1DH

PWM pulse Period control by timer TMR2 and PR2

- The time/counts at the holding register of TMR2
- PWM mode makes the TMR2 effectively function as 10-bit timer because 8-bit timer is concatenated with 2-bit internal prescaler (Q-clock)

TMR2 and PR2 (Period register for timer TMR2 post scaling)

- PWM pulse generates from TMR2
- TMR2 holding register at address 0x11
- TMR2CON control register for TMR2 at address 0x12
- The bits at PR2 used for final PWM period (and thus pulse frequency)

PWM Period

- PR2 register PR2 address 92H
- Let PR2 is written 2-bit value = y
- Let prescale factor = *p*. T
- osc is the period of the oscillator
- PWM period = [y + 1] × 4 × Tosc × *p*
- PWM frequency = 1/ PWM period

PWM Duty Cycle

- PWM duty cycle 8 bits written at CCPR1L
- 2 bits written at CCP1CON bits b5-b4
- CCPR1H is internally loaded from CCPR1L at the reset of TMR2
- Thus double buffering of PWM duty cycle 8-bits
- PWM mode makes CCPR1H as read only register

PWM Period

- PWM period written in PR2 register and TMR2 prescale value
- Enable TMR2 by writing T2CON
- CCP1 Pin made output by clearing bit b2 of TRISC (data direction register for port C)

CP1CON address 0x17 bits at 0x17

- Bit b7-b6 are always 0 (not implemented in 16F877) Bit b5-b4 are not used in PWM mode.
- Bit b3-b2-b1-b0 = 11xx then compare/capture mode disabled and PWM mode enabled
- Bit b5-b4 are lower two bits for the 10-bit PWM duty cycle.
- PWM duty cycle period = (10-bits b5-b4 in CCP1CON-CCPR1L) × Tosc × TMR2 prescaler factor

- When TMR2 = PR2, then on next increment of TMR2 (i) TMR2 resets, (ii) CCP1 pin at RC2 = 1. If PWM duty cycle = 0%, then CCP1 pin is not set. (iii) 8-bits of PWM duty cycle value are latched into CCPR1H from CCPR1L. The time/counts at the holding register of TMR2 are 10-bits at TMR2 + internal prescaler bits. TMR2 8-bits are at address 0x11H. The bits are used for comparing and matching the 10-bits at 2-bits at b5-b4 in CCP1CON and 8-bits in CCPR1H by the CCP1 device when CCP1 PWM mode is enabled.
- The interrupt service routine executes if interrupt is enabled by in SFR PIE1 (peripheral interrupt enable register 1) bit b2 CCP1IE and INTCON PEIE (peripheral-enable interrupts enable) bit b6. PIE1 address is 0x8C. INTCON address is 0x0B/0x8B/0x10B/0x18B. There is no interrupt flag in PWM mode.

Interrupt service routine execution

- if interrupt is enabled by in SFR PIE1 (peripheral interrupt enable register 1) bit b2 CCP1IE and INTCON PEIE (peripheral-enable interrupts enable) bit b6
- PIE1 address at 0x8C
- INTCON address at 0x0B/0x8B/0x10B/0x18B
- No interrupt flag in PWM mode

Summary

We learnt

- PWM output has a time-base period (pulse-period, (total output pulse period for 1 and 0)
- PWM pulse frequency =1/ Pulse period
- PWM output has a duty cycle (the period of output pulse = 1)

We learnt

- PWM1 output on integration generates an analog output1, linearly related to bits in a register CCP1L andCCP1CONb5-b4
- PWM2 output and Analog output2 relate to CCP2L and CCP2CONb5-b4

We learnt

- 10-bit Duty cycle value of PWM1 controlled by CCP1L 8-bit and CCP1CON bits b5-b4
- 10-bit Duty cycle value of PWM2 controlled by CCP2L 8-bit and CCP2CON bits b5-b4

We learnt

- 10-bit pulse period controlled by TMR2 and PR2 for both PWM1 and PWM2

End of Lesson 12 on

Pulse Width Modulation Outputs 1 and 2 using CCP1 and CCP2