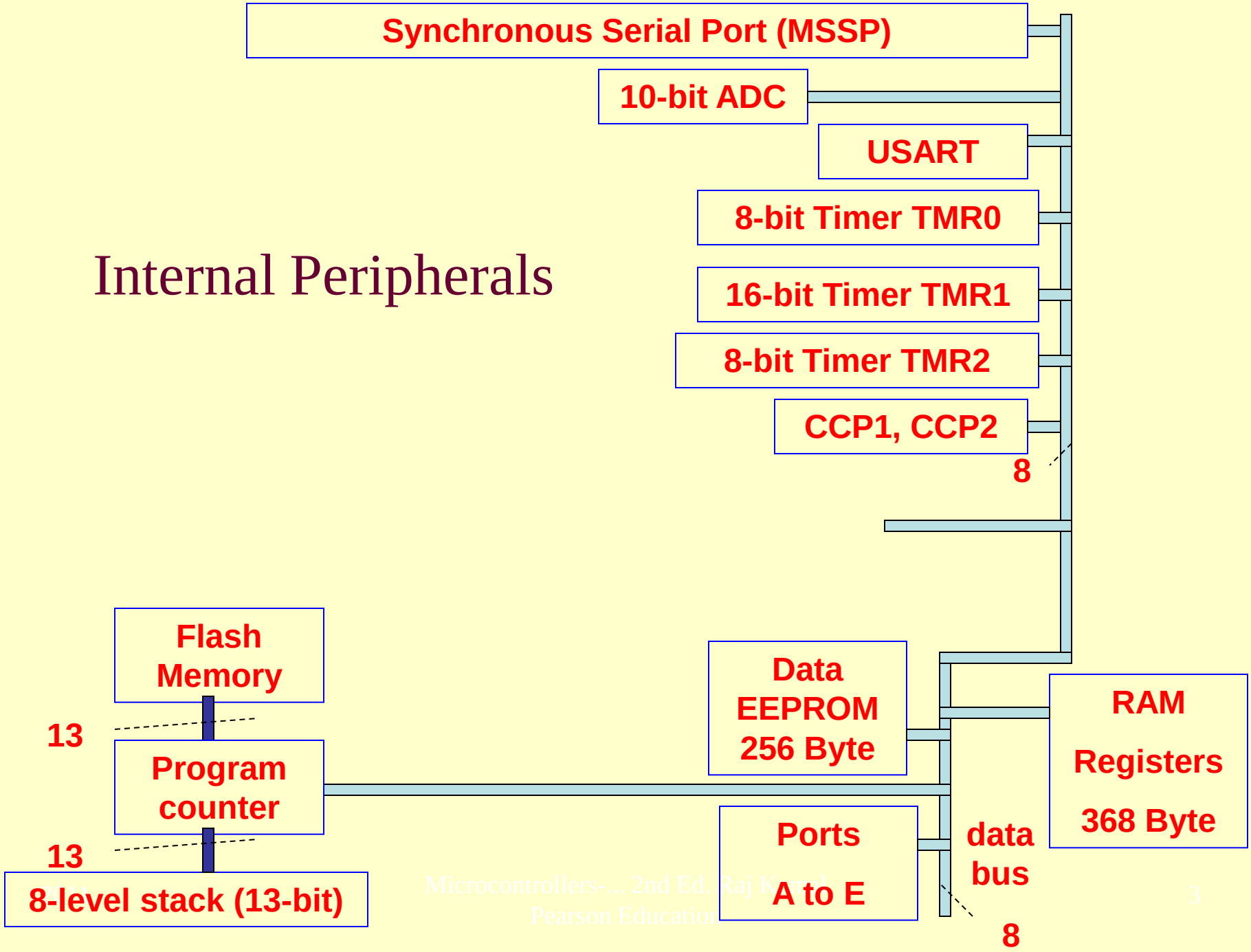
Chapter 13

PIC Family Microcontroller

Lesson 10

Compare Outputs and Interrupts using CCP1 and CCP2

Internal Peripherals



CCP1 Compare Mode

- 16-bit in compare mode of CCP1 registers CCPR1H: CCPR1L
- Written and read using address 0x16 and 0x15 (bank 0 SFRs)
- CCP1 control register CCP1CON
- It is written or read using 0x17H

CCP1 Compare Mode

- Use 16-bit timer TMR1 for comparison
- The time/counts at the holding register of TMR1— 16-bits at TMR1H:TMR1L
- TMR1H:TMR1L at address 0x0F-0x0E
- The bits are used for comparing and matching the 16-bits at CCPR1L:CCPR1H by the CCP1 device when CCP1 compare mode enabled
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CCP2 Compare Mode

- CCPR2H:CCPR2L 16-bit used in compare mode of CCP2
- Written and read at address 0x1C and 0x1B (bank 0 SFRs)
- CCP2 control register CCP1CON
- Written or read using 0x17H

CCP2 Compare Mode

- 16-bits at TMR1H:TMR1L time/counts at the holding register of TMR1
- Address 0x0F-0x0E
- TMR1H:TMR1L Bits used for comparing and matching the 16-bits at CCPR2L:CCPR2H by the CCP2 device when CCP2 compare mode enabled

Using the CCP1CON bits at 0x17

- Bit b7-b6 always 0 (not implemented in 16F877)
- Bit b5-b4 are not used in compare mode
- Bit b3-b2-b1-b0 = 1111 then compare/capture/PWM mode disabled
- = 1000 then compare mode activated. CCP1 device sets an output on *match* (means TMR1H:TMR1L counts have become equal to CCPR1L:CCPR1H). A flag CCP1IF (CCP1 interrupt flag) is also set. The output is at pin CCP1 (pin RC2 of PORTC).

Using the CCP1CON bits b3-b2-b1-b0 = 1000

- Compare mode activated
- The output at pin CCP1 (pin RC2 of PORTC) set *on match*
- CCP1 device sets an output on *match* (means TMR1H:TMR1L counts have become equal to CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also set
- The output at pin CCP1 (pin RC2 of PORTC)

Using the CCP1CON bits b3-b2-b1-b0 = 1001

- Compare mode activated
- The output at pin CCP1 (pin RC2 of PORTC) reset *on match*
- CCP1 device clears the output on *match* (means TMR1H:TMR1L counts have become equal to CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also set
- The output at pin CCP1 (pin RC2 of PORTC)

Using the CCP1CON bits b3-b2-b1-b0 = 1010

- If = 1010 then compare mode software timer mode activated
- Means the output at pin CCP1 (pin RC2 of PORTC) not changed
- CCP1 device generates software interrupt *match* (means TMR1H:TMR1L counts have become equal to CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also set

Using the CCP1CON bits b3-b2-b1-b0 = 1011

- Compare mode special event trigger mode activated
- The output at pin CCP1 (pin RC2 of PORTC) is not changed.
- CCP1 device generates reset for TMR1 on *match* (means TMR1H:TMR1L counts have become equal to CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also set

CCP1IF (CCP1 interrupt flag)

- SFR PIR1 (peripheral interrupt register 1) bit b2
- PIR1 address 0x0C
- When CCP1IF (CCP1 interrupt flag) set, the interrupt service routine executes

Interrupt Execution on CCP1IF (CCP1 interrupt flag) Setting

- Execution if interrupt enabled by in SFR PIE1 (peripheral interrupt enable register 1) bit b2 and INTCON PEIE (peripheral-enable interrupts enable) bit b6
- PIE1 address is 0x8C
- INTCON address is 0x0B/0x8B/0x10B/0x18B.

CCP2CON Bits

- CCP2CON bits at 0x1D are used as follows:
- Bit b7-b6 are always 0 (not implemented in 16F877)
- Bit b5-b4 are not used in compare mode
- B3-B2-B1-B0 used
- Bit b3-b2-b1-b0 = 1111 then compare/capture/PWM mode disabled.

CCP2CON Bit b3-b2-b1-b0 = 1000

- Compare mode activated
- The output at pin CCP2 (pin RC1 of PORTC) set on match
- CCP2 device sets an output on *match* (means TMR1H:TMR1L counts become equal to CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) set

CCP2CON Bit b3-b2-b1-b0 = 1001

- If = 1001 then compare mode activated
- The output at pin CCP2 (pin RC1 of PORTC) reset on match
- CCP2 device clears the output on *match* (means TMR1H:TMR1L counts have become equal to CCPR2L:CCPR2H).
- A flag CCP2IF (CCP2 interrupt flag) also set

CCP2CON Bit b3-b2-b1-b0 = 1010

- If = 1010 then software timer mode of compare option activated
- The output at pin CCP2 (pin RC1 of PORTC) is not changed
- CCP2 device generates software interrupt *match* (means TMR1H:TMR1L counts have become equal to CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) is also set

CCP2CON Bit b3-b2-b1-b0 = 1011

- Compare mode special event trigger mode activated
- The output at pin CCP2 (pin RC1 of PORTC) not changed
- CCP2 device starts AD conversion if ADC device activated

CCP2CON Bit b3-b2-b1-b0 = 1011

- CCP2 device generates reset of TMR1 counts on *match* (means TMR1H:TMR1L counts have become equal to CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) also set

CCP2F (CCP1 interrupt flag)

- SFR PIR2 (peripheral interrupt register 2 bit b0. PIR2 address 0x0D
- When CCP2IF (CCP2 interrupt flag) set, the interrupt service routine executes

CCPR2 Interrupt Service Routine Execution

- If interrupt is enabled by in SFR PIE2 (peripheral interrupt enable register 2) bit b0 and INTCON PEIE (peripheral-enable interrupts enable) bit b6
- PIE2 address is 0x8D
- INTCON address 0x0B/0x8B/0x10B/0x18B

Summary

We learnt

- CCP1 and CCP2 Compare Modes
- Four Options Each

(i) Set Output at an RC pin and also Interrupt Flag set on match

(ii) Reset Output at RC pin and also Interrupt Flag reset on match

(iii) No change in Output at RC pin and Interrupt Flag reset on match

We learnt

(iv) TMR1 16-bit counts resets and Special Event Trigger Mode activates

End of Lesson 10 on

Compare Outputs and Interrupts using CCP1 and CCP2