Chapter 13

PIC Family Microcontroller

Lesson 06

Special Function Registers for Control and status registers for the peripherals, input/output and Interrupt

SFRs

- SFRs at the addresses of internal RAM/register file for the GPRs (general purpose registers)/RAM)
- Starting from 0x0000 and 0x000 (Data memory)
- An SFR accessed by 7-bit direct address or 8-bit indirect address at FSR

SFR Banks

- Register file of 256 bytes in 4 banks (two bank-pairs)
- Each bank of 128 byte and registers/RAM has the data at 7-bit addresses 0x00 to 0x7F in a bank.
- Bank base address starts from address 0x08 × bank number (0 or 1 or 2 or 3). [Lower addresses in a bank are for the SFRs. Higher addresses are for the GPRs

SFR space

32 B in Bank 0	0x00H-0x1F
32 B in Bank1	0x80H-0x9F
16 B in Bank2	0x100H-0x10F
16 B in Bank3	0x180H-0x18F

Frequently used SFRs Mirroring in all four banks

- PCL, STATUS, FSR, PCALTH and INTCON Mirrored in four banks
- Some SFRs mirrored in two bank-pairs (bank-pair 0 and 1)
- TMR0 (timer TMR0) mirrored in a banks 0 and 2 (bank-pair 0 and 1)

Mirroring in all four banks

- OPTION_REG mirrored in banks 1 and 3 (bank-pair 0 and 1)
- PORTB mirrored in bank 0 and 2 (bank-pair 0 and 1).
- TRISB (transmit/receive input/send bit) mirrored in bank 1 and 3(bank-pair 0 and 1)

Frequently used SFRs Mirroring in both bank-pairs

- Some SFRs mirrored in two bank-pairs (bank-pair 0 and 1)
- TMR0 (timer TMR0) mirrored in a banks 0 and 2 (bank-pair 0 and 1)

Example

- SFR PCL address 0x02H
- Mirrors in all the four banks
- Can also be accessed from any bank 0 or 1, 2 or 3 using address 0x02H

Example

- SFR TMR0 address 0x01/0x101 in bank 0 and 2
- TMR0 (timer TMR0) mirrored in bank 0 and 2
- Can also be accessed from any bank-pair 0 or 1 using address 0x01
- Bank pair 1 base address 0x100

SFR OPTION_REG Mirroring

- OPTION_REG is mirrored in bank 1 and 3
- Address 0x81/0x181 in bank 1 and 3
- Can also be accessed from any bank-pair 0 or 1 using address 0x81
- Bank pair 1 base address is 0x100

SFR STATUS Mirroring

- Address 0x03H
- Mirrors in all the four banks
- Can also be accessed from any bank 0 or 1, 2 or 3 using address 0x03H.

Bank0 SFRs

IndirectAddr	TMR1L, TMR1H and T1CON
TMR0	TMR2, T2CON
PCL	SSPBUF, SSPCON
STATUS	CCPR1L-CCPR1H, CCP1CON
FSR	RCSTA
PORTA	TxREG
PORTB	RCREG
PORTC, D	CCPR2L-CCPR1H, CCP1CON
PORTE	ADRESH
PCLATH (PC address translation higher bits)	ADCON0
INTCON	
PIR1, PIR2	

Bank1 SFRs

IndirectAddr	PCLATH
OPTION_REG	INTCON
PCL	PIE1, PIE2
TRIS C TRIS D	PCON
TRISE	SSPCON2
	PR2
STATUS FSR TRISA TRISB	SSPADD-SSPSTAT, CCP1CON
	TxSTA
	SPBRG
	ADRESL
	ADCON1

Bank2 SFRs

IndirectAddr
TMR0
PCL
STATUS
FSR
PORTB
PCLATH
INTCON
EEDATA
EEADDR
EEDATH
EEADRH

Bank3 SFRs

IndirectAddr
OPTION_REG
PCL
STATUS
FSR
TRISB
PCLATH
INTCON
EECON1, EECON2

Summary

We learnt

- 32 SFRs Space in Bank 0
- 32 SFRs Space in Bank 1
- 16 SFRs Space in Bank 2
- 32 SFRs Space in Bank 3
- Mirroring of Certain commonly used SFRs in all banks
- Mirroring of Certain commonly used SFRs in both bank pairs

We learnt

- SFRs accessible at Bank 0
- SFRs accessible at Bank 1
- SFRs accessible at Bank 2
- SFRs accessible at Bank 3

End of Lesson 06 on

Special Function Registers for Control and status registers for the peripherals, input/output and Interrupt