Chapter 13

PIC Family Microcontroller

Lesson 04

Memory

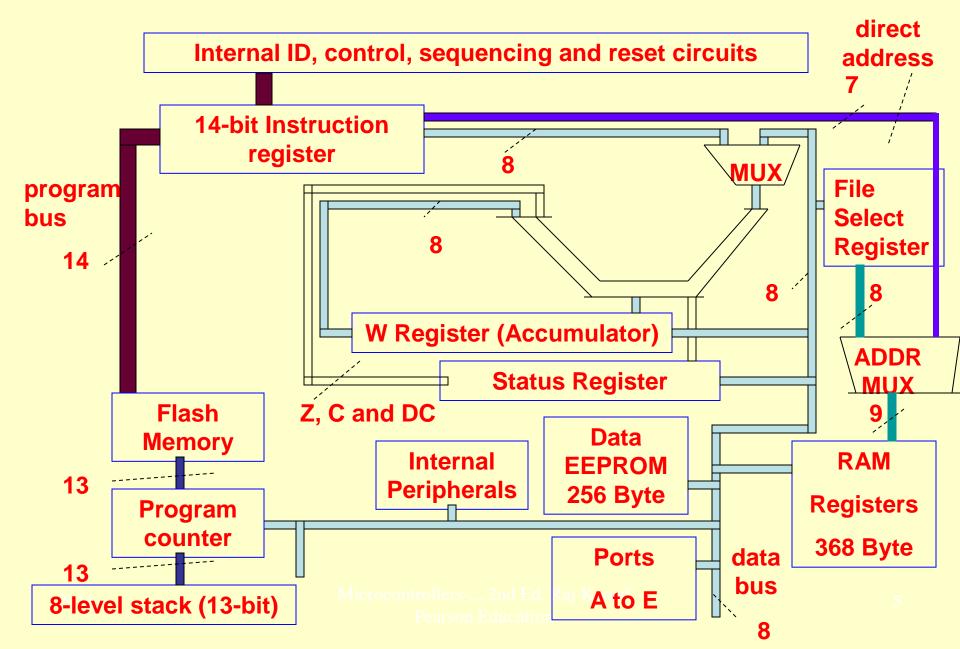
On-Chip Memory for Data

- SFRs (Special Function Registers)
- GPRs (General Purpose Registers)
- Internal RAM
- Data EEPROM

On-Chip Memory for Program

• Program memory (Flash)

Internal hardware for the operations in a PIC family MCU



Special Function Registers

- Control and status registers for the peripherals, input/output and Interrupt
- These are at direct as well as indirect addressable memory area for the register file
- SFR space is 32 B in Bank 0,
- 32 B in Bank1,
- 16 B in Bank2 and
- 16 B in Bank3.

General Purpose registers for the read and write

- GPRs/ Internal Random Access memory; total 352 byte space.
- Highest 16B RAM addresses in each bank are common to all other banks.
- 96 B in Bank 0,
- 96 B in Bank 1,
- 80 B for Bank 2 and
- 80 B for Bank 3 memory space is for the GPRs/ Internal Random Access memory

256-byte EEPROM for Data in 16F877

- Read and write are through six SFRs. [EECON1 and EECON2, EEADRH-EEADR and EETATH-EEDATA]
- EEPROM Write operation means erase and then write
- Stores run-time generated and updated values
- Values non-volatile (don't change on power down)

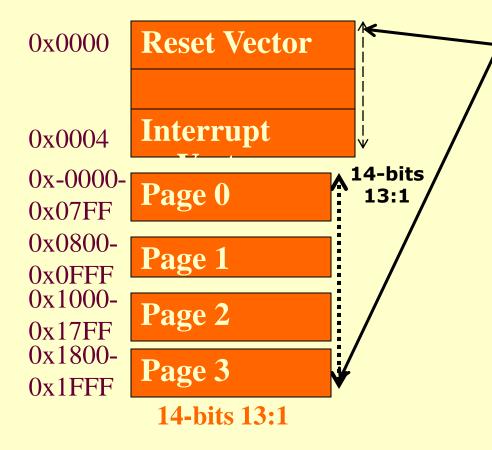
Program Memory in Flash

- A write operation means erase and then write
- Program memory can store instructions, constant data, calibration parameters, ASCII text etc
- Fetch and access to invalid instruction results execution of NOP (no operation)

Access to program memory in 16F877 $(8 \text{ k} \times 14 \text{ flash version})$

- Allows for check-sum calculations
- Read and write is through six SFRs [EECON1 and EECON2, EEADRH-EEADR and EETATH-EEDATA]
- 14-bit data for write is placed at EEDATH-EEDATA.
- EEADRH-EEADR 13-bit address The valid program memory addresses are between 0x0000 and 3FFF

Program Memory Map	
2000H-2013H	Lower Table of Interrupt Vectors
2018H	Config byte
2018-2FH	Security Key ROM/EPROM
2030-3FH	Upper Table of Interrupt Vectors
2040-5DH	Peripheral Transactions Server
2080H-	Vectors
5FFFH	User Program, constants,
	stored tables



8-level stack, onto which PC is pushed on CALL instruction and is popped on Return, Return from interrupt or return of a long word 13-bit program counter 12:1ID locations (read or write

when programming or verifying) 0x2000-0x2004

Configuration word 0x2007

Configuration word 0x2007

Summary

We learnt

- Data Memory
- SFRs (Special Function Registers)
- GPRs (General Purpose Registers)
- Internal RAM
- Data EEPROM

We learnt

- Program memory (Flash)
- 13-bit program counter
- 14-bit instructions
- Reset Vector
- Interrupt Vectors
- Pages 0, 1, 2 and 3 up to 0x1FFF (8 k) 14-bit at each address

We learnt

- 0x2000 onwards
- ID locations
- Configuration word
- Program Codes
- 8-level stack 13-bit

End of Lesson 04 on

Memory