Chapter 13

PIC Family Microcontroller

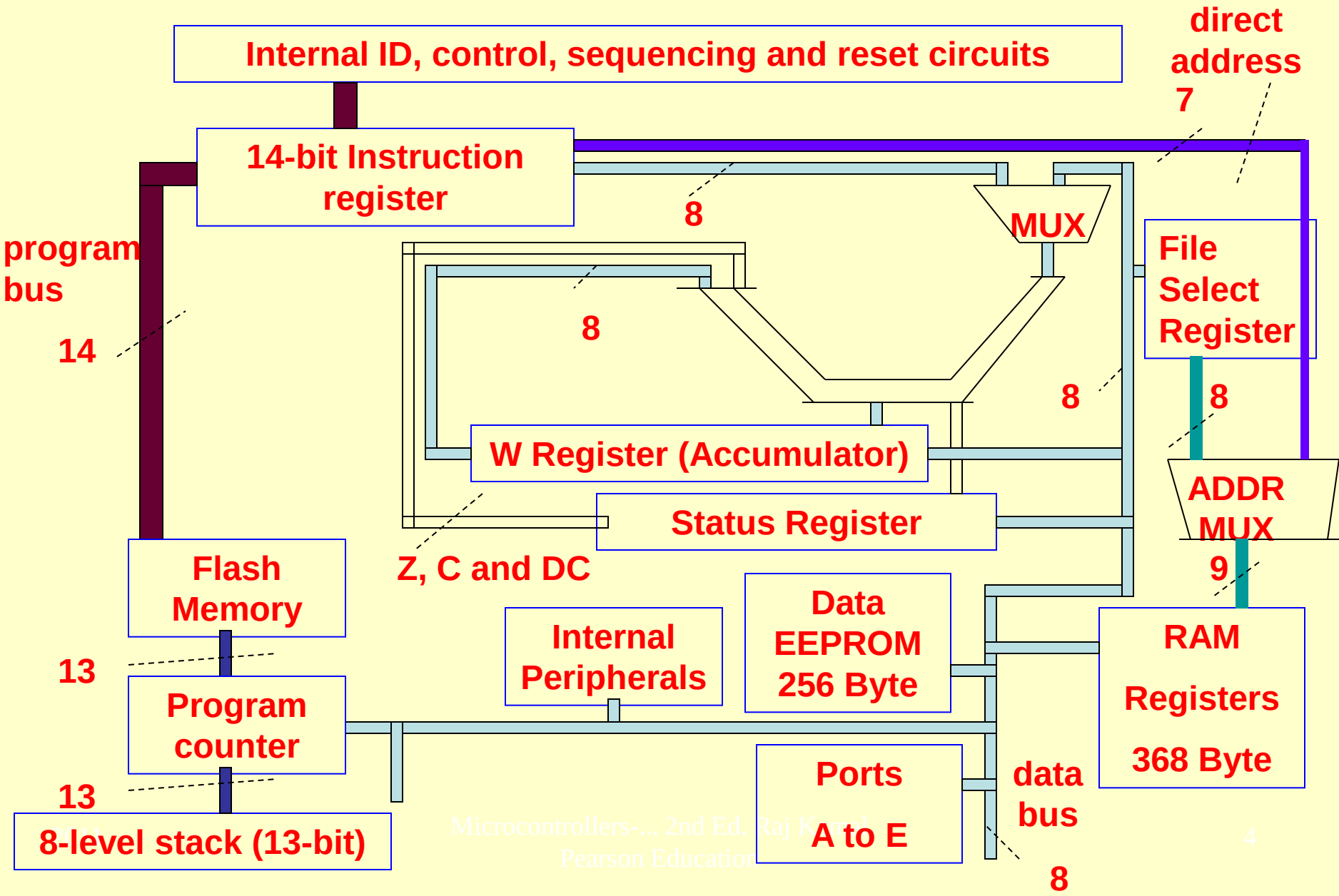
Lesson 03

Register File

Register file/RAM

- Saves 368 B in PIC 16F877.
- 9-bits of address required to access the file/RAM
- Register file/RAM divides in four banks
- Each bank has 128 addresses.
- Each bank register/RAM therefore accesses by 7-bit address (called direct address)
- Bank is decided for the access by the RP1:RP0 bits

Internal hardware for the operations in a PIC family MCU



Bank 7-bit Address

- 7-bit address is used when using direct address for a register/RAM in an instruction [Instruction has 14-bits.]
- This address plus the bank base address generates 9-bit address of a register/internal RAM
- Bank Base Address is as per RP1:RP0 bits.

Four **banks** of Registers/RAM

- The register/RAM in bank 0 at address between 0x000 and 0x07F
- The register/RAM in bank 1 at address between 0x080 and 0x0FF
- The register/RAM in bank 2 at address between 0x100 and 0x17F
- The register/RAM in bank 3 is at address between 0x180 and 0x1FF.

Example

- A byte at an address 0x25 accessed directly by using direct address 0x25 in the instruction
- . It is considered at bank 0 as 0x25 falls in bank 0 address space.

Direct Address

- A byte at an address 0x85 can be accessed by 7-bit direct address = 0x05 of Bank 1
- [Bank 1 base address is 0x80 and 0x85–0x80 = 0x05

Bank Pairs

- Four banks form two pairs of banks of Registers/RAM
- The register/RAM in lower bank pair is at address between 0x000 and 0x0FF
- A Bank pair needs 8-bit to access.
- The register/RAM in upper bank pair is at address between 0x100 and 0x1FF
- Bank-pair 0 address is 0x000 and 1 address is 0x100.

Register/RAM Bank Pair access

- By 8-bit address
- Bank pair is as per IRP bit
- 8-bit address is used when using indirect address for a register/RAM
- This address plus the bank-pair base address generates 9-bit address of a register/internal RAM
- Bank pair base address is as per IRP.

RAM/File Register Select Register (FSR)

- FSR is used for indirect addressing in the instruction
- FSR of 8-bits
- It provides the 8-bit address of RAM/register in register file
- That address is in a bank-pair
- Bank pair is as per IRP bit in the STATUS.

ADDRMUX

- Address multiplexer generates 9-bit address for accessing register file/RAM
- ADDRMUX is given input either by 7-bit direct address in the instruction or by 8-bit indirect address from FSR.
- 9-bit address from ADDRMUX s as per Plus RP1:RP0 bits or IRP at STATUS Register

IRP (indirect register-bank pair) bit

- Indirect address has 8-bits.
- These bits are taken from either lower pair of banks 0 or 1 or upper pair of banks 2 or 3
- Bit 7 in STATUS, when = 1, then upper bank-pair used
- When = 0 then lower bank pair used.

RP1-RP0 (register- pair higher bank-register pair lower bank) bits

- Direct address has taken from 7-bits in the instruction
- They are taken for either bank 0 or 1 or 2 or 3.
- Bit 6-5 in STATUS, when = 11, then higher bank 3. When = 10, then bank 2. When = 01, then bank 1. When = 00, then bank 0.

Higher addresses Mirroring in all four banks

- Higher addresses 0x70-0x7F in a bank are also mirrored.
- When 0x70-0x7F is accessed, then it also means access to 0xF0H-0xFFH, 0x170-0x17F and 0x1F0-0x1FF.
- Frequently used variables are stored at these sixteen addresses by the programmer

Summary

We learnt

- Register File/RAM 368 Bytes
- 9-bit address
- Address generates by 7-bit direct address in the instruction or
- Address generates by 8-bit indirect address in in File Select Register
- Register file of 368 bytes divides in four banks
- Bank has 128 bytes each

We learnt

- Bank base address is as per RP1:RP0 bits in STATUS register
- Register file of 368 bytes divides in two bank-pairs
- Bank pair has 256 bytes each
- Bank pair base address as per IRP bit in STATUS register
- Higher addresses Mirroring in all four banks for frequently used variables are stored

End of Lesson 03 on

Register File