Chapter 7

System Design: Peripheral ICs and Interfacing

Lesson 7

I²CBus Interface

Serial Bus

- Serial bus connects several devices through common lines

- Only addressed device receives (accepts) the line output from communication device at an instance

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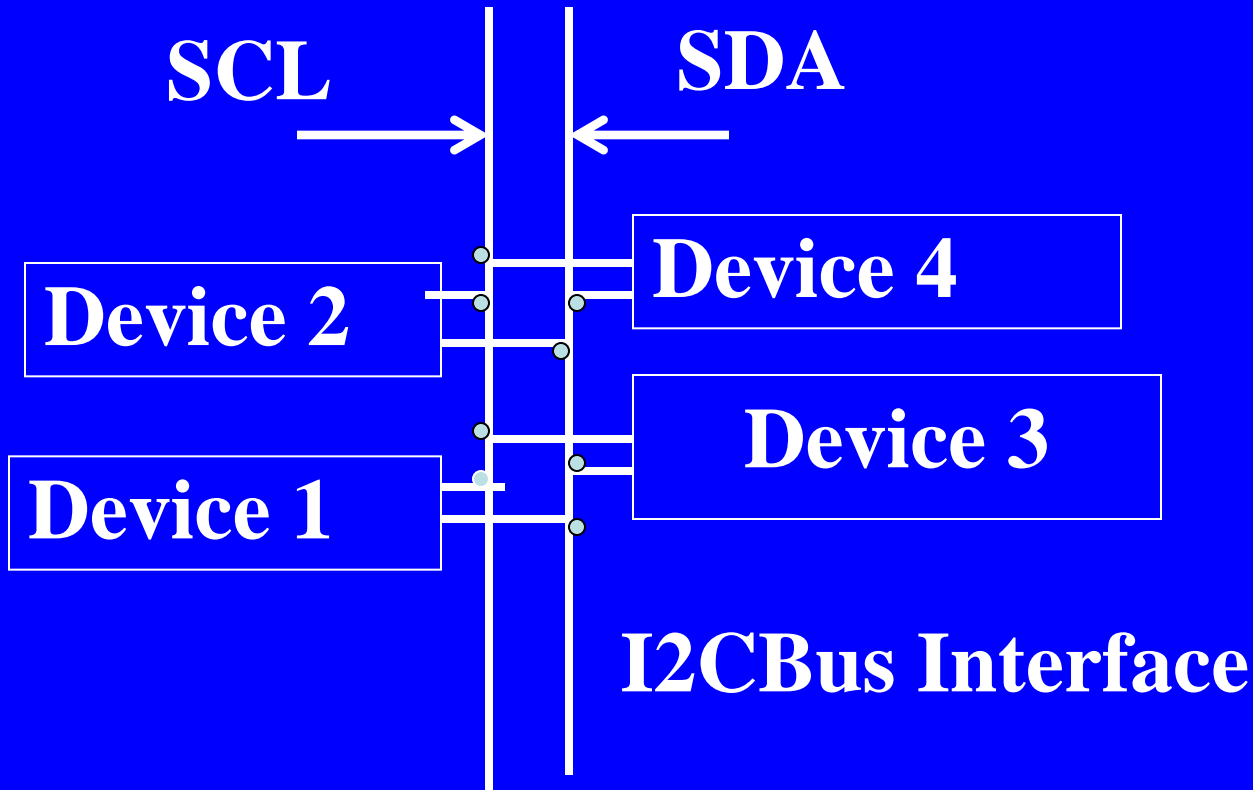Pearson Education

Serial Bus

- Communicates bits for data and protocol bits at a defined rate

- Some Protocol related bits precede the data bits

- Some Protocol related bits succeed the data bits

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clock line   **Serial Data line**

SCL   **SDA**

Device 4

Device 2

Device 3

Device 1

I2CBus Interface

8051 MCU with I²C
SCL (P1.6) and SDA (P1.7) signals

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Master-Slave Communication

• Master at I^{2}C serial synchronous bus sends clock pulses SCL and data bits SDA

• Slave receives bits after synchronizing the SCL clock

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Start bit

Slave address   data bits or command

specify read/write

NACK   Stop

specify ack

| b0 | b1-b7 | b8 | b9 | b10-b17 | b18 | b19 |
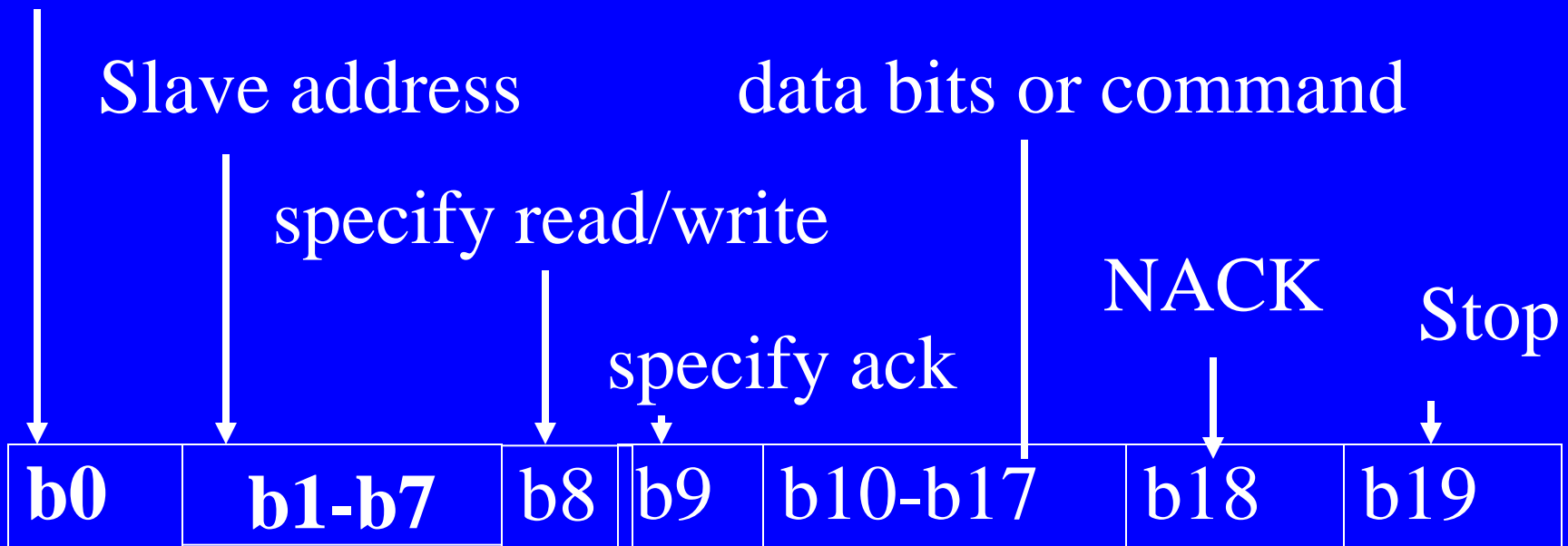
I^{2}C Bus Protocol and Data Serial line bits

SDA (Serial Data) line in I²C

Start bit

Stop

0 0 1 0 0 0 1 0

slave address = 34

data bits 69H

Data bits (10100100) 20T format

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Timings of Ten clock pulses

SCL at slave address

start bit

| 0 |

clock pulse width = 4.7 μs

clock pulse 0 for 1.3 μs min.

SCL(Serial Clock) serial line in I^2C

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Summary

We learnt

I^{2}C

- A serial synchronous bus -two lines SCL and SDA

- Interconnects 128 devices

- 20 bits per byte communication

- Start and stop bits

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