# Chapter 7

# System Design: Peripheral ICs and Interfacing

# Lesson 4

## 8259- Programmable Interrupt Controller

# Programmable Interrupt Controller 8259 Features

- 8 External interrupt requests with priority levels 0-7 extendable to 0-63 by cascading

- Each request separately maskable

- TTL level output compatible with Intel processors

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# 8259 Features

- Priority Resolver

- 8 External interrupt requests normal priorities: IRQ0highest, IRQ7 lowest

- Each request separate mask bit

- Each request separate level of interrupt

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# 8259 Features

- 8259 if set in 8086 processor mode, then sends the level to 8086 of an Interrupt request from peripheral

- 8086 interrupt level defines by a byte having value between 0 and 255

- The level multiplies by 00004H to define a vector address

- Vector address is used by processor to fetch the CS and IP for an Interrupt service routine

- ISR needed for servicing a interrupt request

# 8259 Features

- 8259 if set in 8085 processor mode, then sends 1st fetched byte by 8085 from 8259— a code for instruction (jump code or call code)

- 2nd and 3rd fetched bytes in 2nd and 3rd Interrupt ACK cycles from 8259—address 16-bit word

- The address defines a vector address for the Interrupt service routine

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# Priorities Resolution at 8259 among interrupt requests from peripherals

# ICW4 (an initial command word) for programming priority resolution by 8259 priority resolver

1. Nested mode for priority resolver

2. Automatic mode for priority resolver

3. Specific rotation mode for priority resolver

# Nested mode

IRQ0 Highest, IRQ 7 lowest

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# Auto or Specific rotation mode for priority resolver

Auto rotate,any IRQ after the service becomes of lowest priority

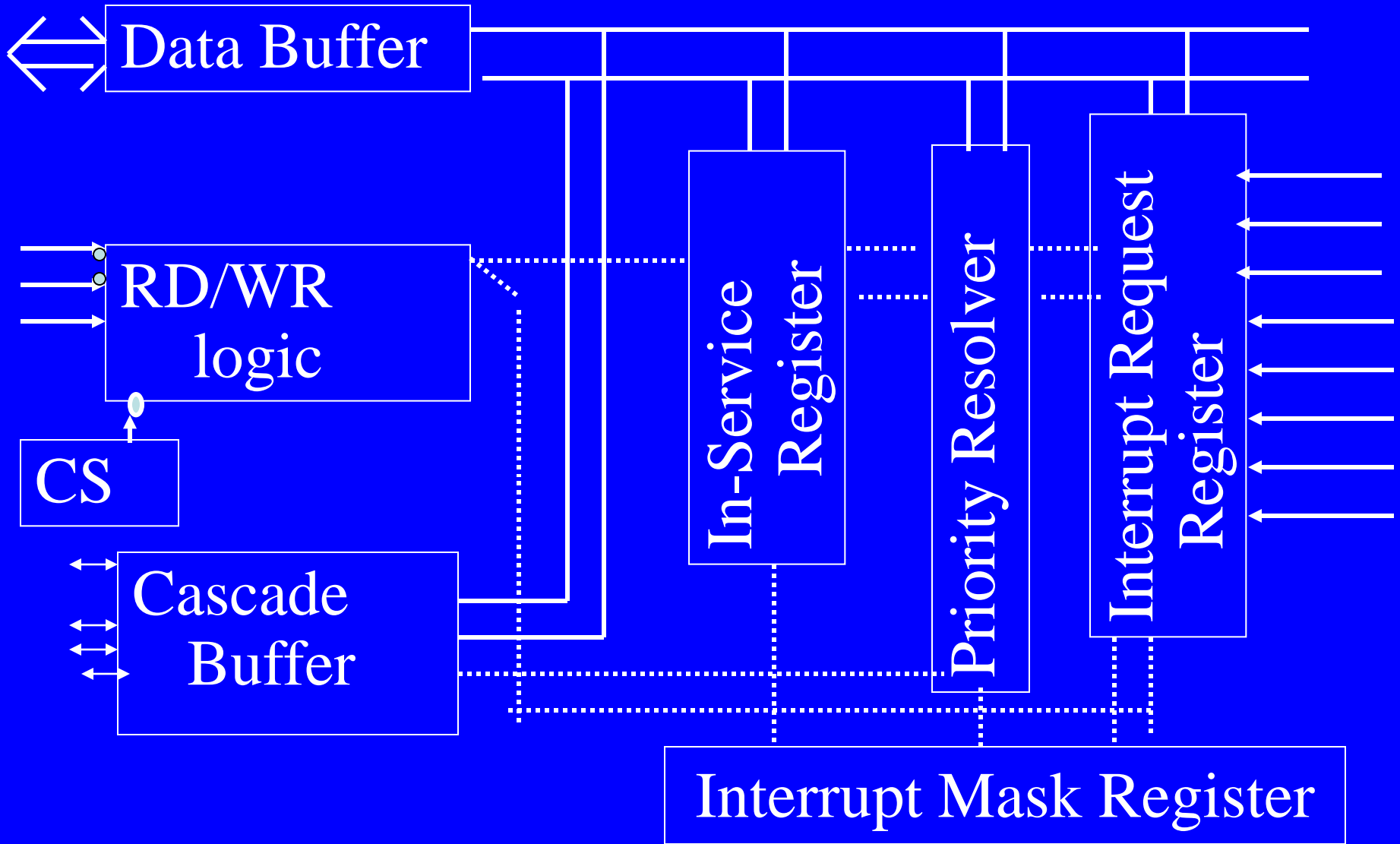Specific rotate, change priority by defining a device of lowest priority, next to it will be highest.

Let us define IR3 lowest. Priorities are now IRQ4, 5, 6, 7, 0, 1, 2, 3

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# In Service register

- Define whether an IRQ serviced or being serviced.

- b7 = 1 means IRQ7 request pending and is being serviced

- 0 means serviced and not pending the service

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# 8259 Block Diagram, Pins and Interfacing

# 8259

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

8259

$\overline{CS}$
$\overline{IOWR}$
$\overline{IORD}$
D4-D0
CSA0
CSA1
GND

VCC
A0
$\overline{INTA}$
IRQ7-0
INTR
$\overline{SP}/\overline{EN}$
D5-D7

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education
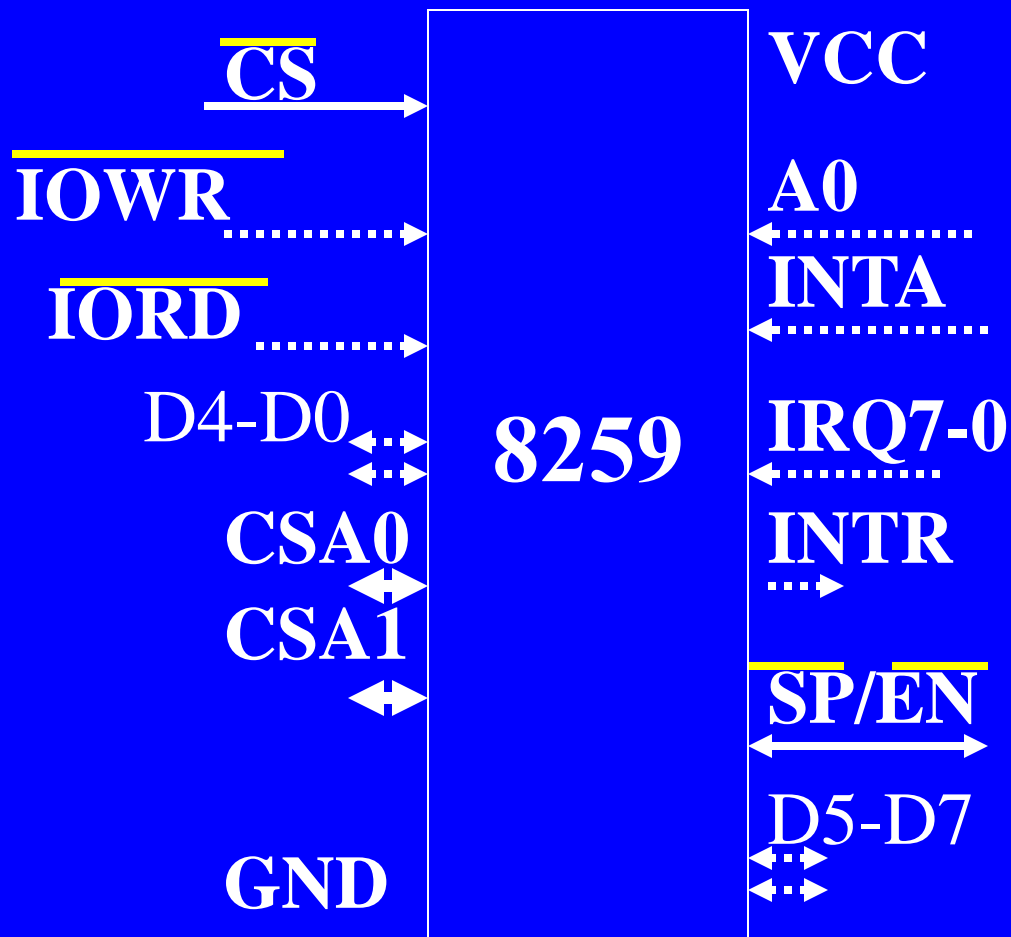
# Table 7.16 - Block Functions

# Table 7.17 - Each Pin signals

**VCC**

**CS**

**IOWR...**

**IORD**

**8259**

**D7-D0**

**CSA0**

**CSA1**

**CAS2**

**GND**

**A0**

**INTA**

**IRQ7-0**

**INTR**

**SP/EN**

**Decoder**

**A1-An**

**AD0 to AD7**

**Latch**

**ALE**

**A0 to An**
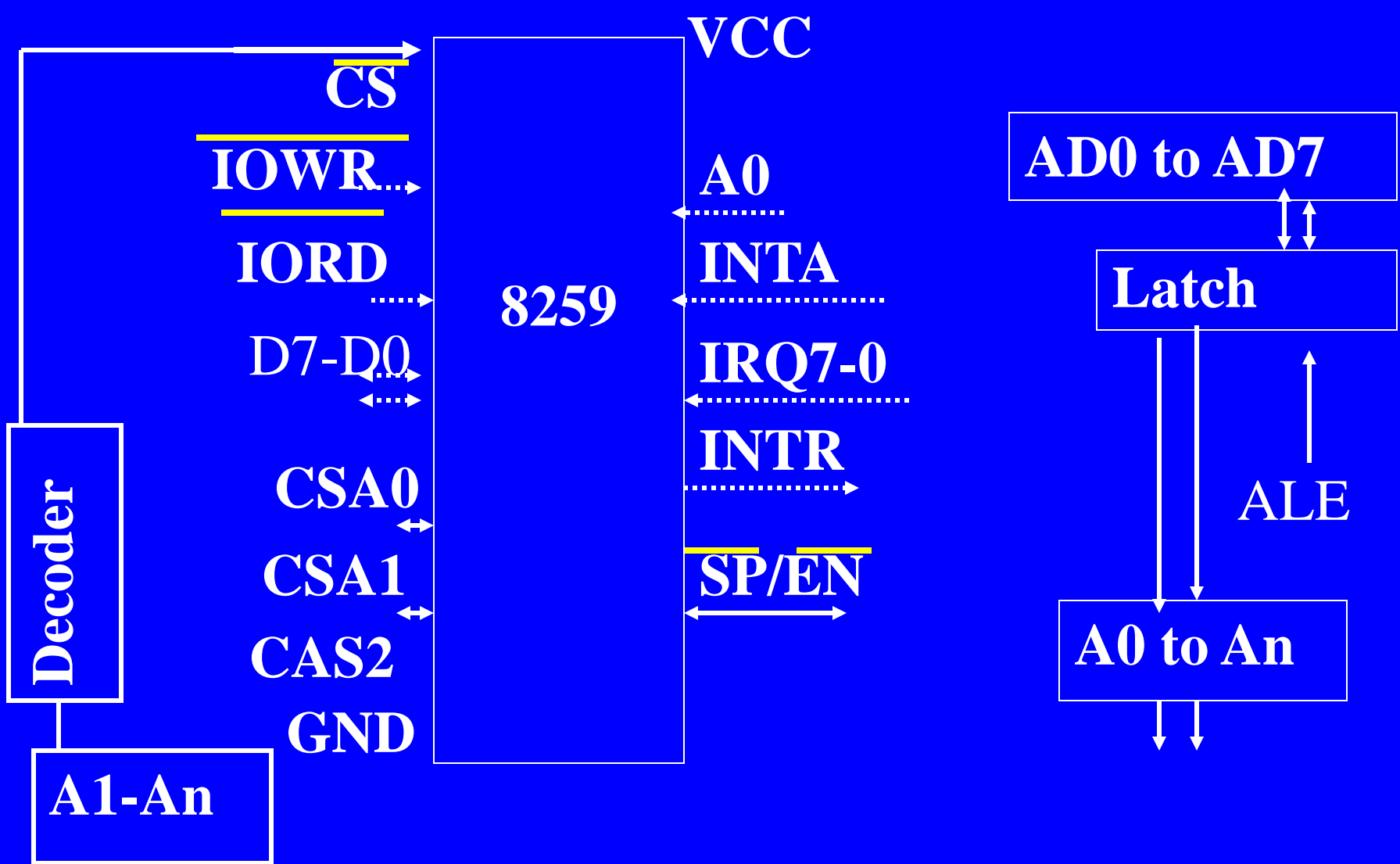
$(\overline{\text{WR}}, \overline{\text{IOWR}}$ or P3.7) and $(\overline{\text{RD}}, \overline{\text{IORD}}$ or P3.6) or R/$\overline{\text{W}}$ and NOT(R/$\overline{\text{W}}$) to $\overline{\text{IOWR}}$ and $\overline{\text{IORD}}$

# Table 7.18 - Exemplary Addresses

20H

Initial Command Word ICW1 and sequences of types for IRQ0-7

21H

Initial Command Words ICW2, ICW3 and ICW4

# Figure 7.14 for details

# 8259 Programming

1. ICW1 Programming is for defining the interrupt levels for each IRQ

2. ICW2 programming is for cascade or normal mode

3. ICW3 programming for automatic or manual end of interrupt

4. ICW4 for programming nested or specific rotation or automatic mode for priority resolver

# Summary

Microcontrollers-... 2nd Ed. Raj Kamal
Pearson Education

# We learnt

- 8259 Programmable Interrupt Controller
- Masks for requests(interrupts) programmable
- Priorities for requests(interrupts) programmable
- Programmable interrupt service routine vectors for an 8-bit level or 16-bit address for each request