Chapter 7

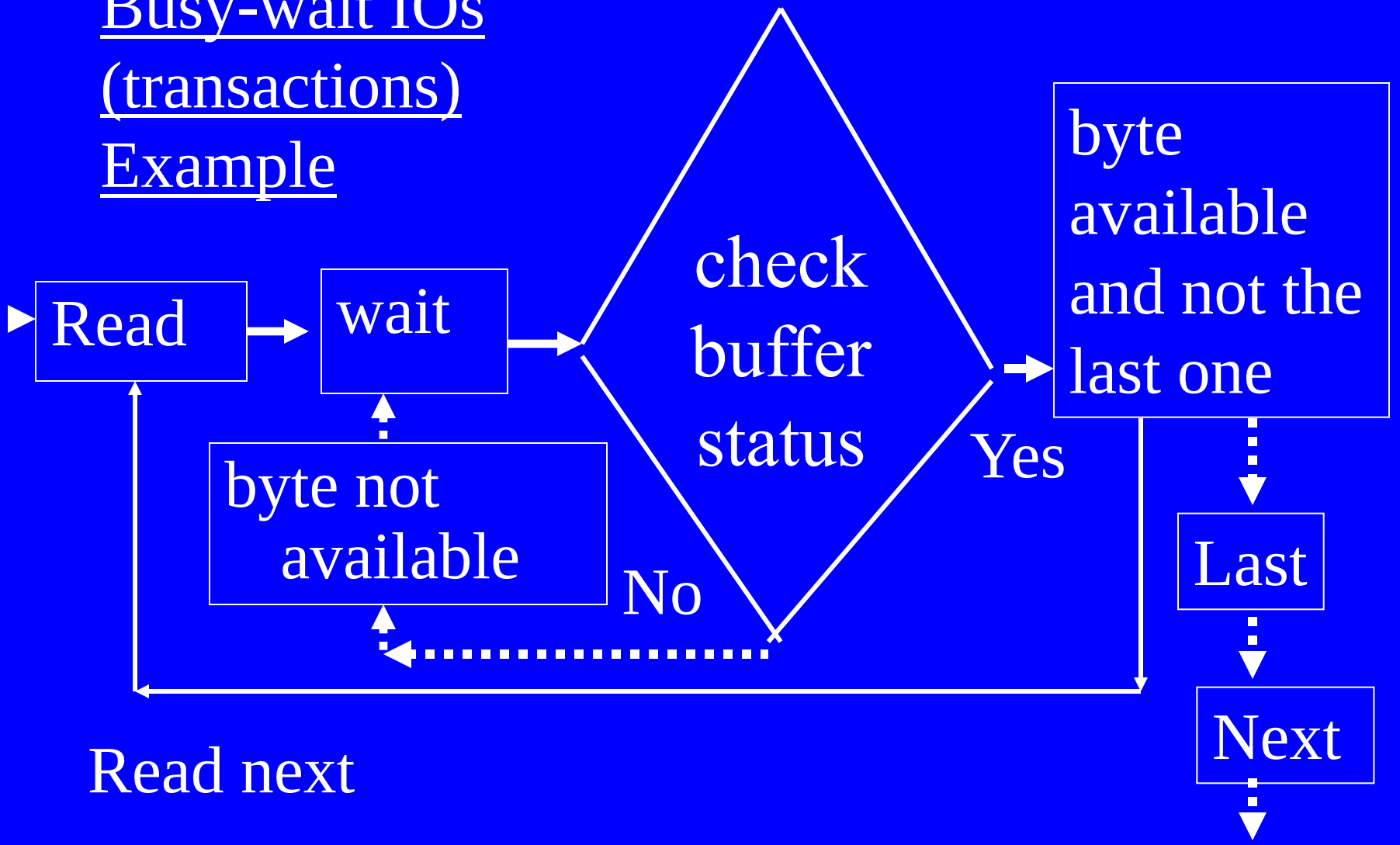
System Design: Peripheral ICs and Interfacing

Lesson 3

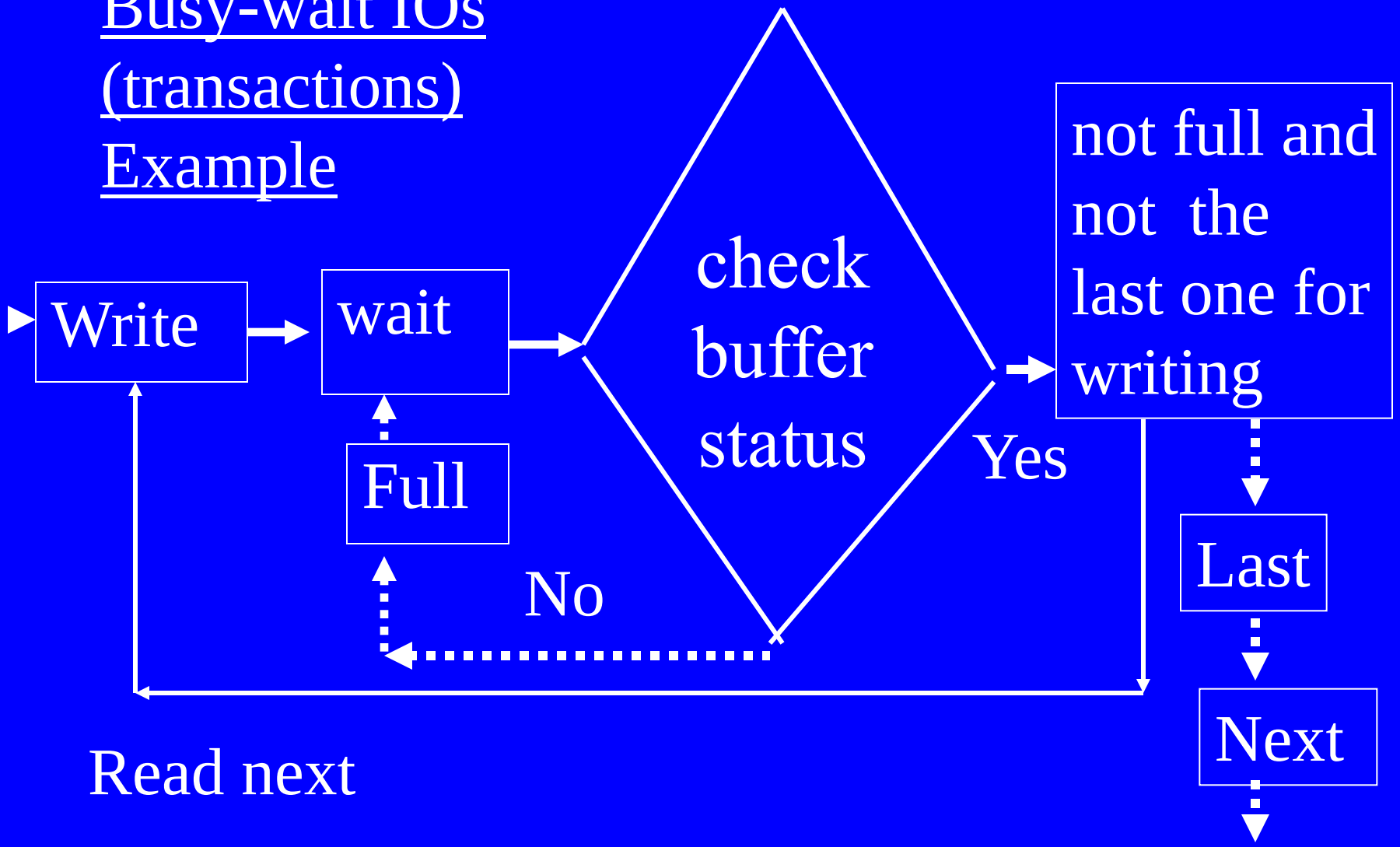
8257- DMA Controller

Three Transaction Methods of IOs for Peripherals

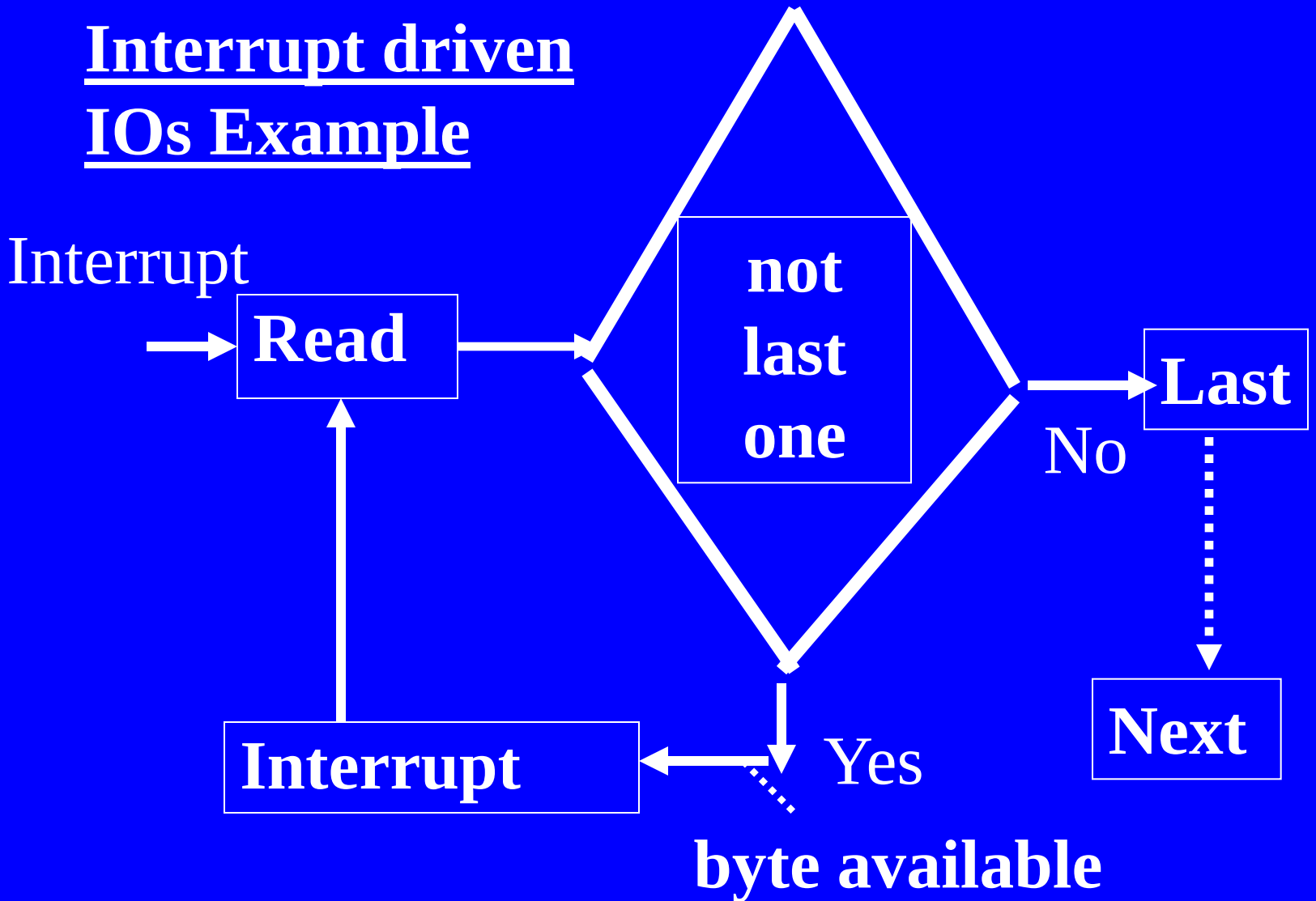
Busy-wait IOs (transactions) Example



Busy-wait IOs (transactions) Example



Interrupt driven IOs Example



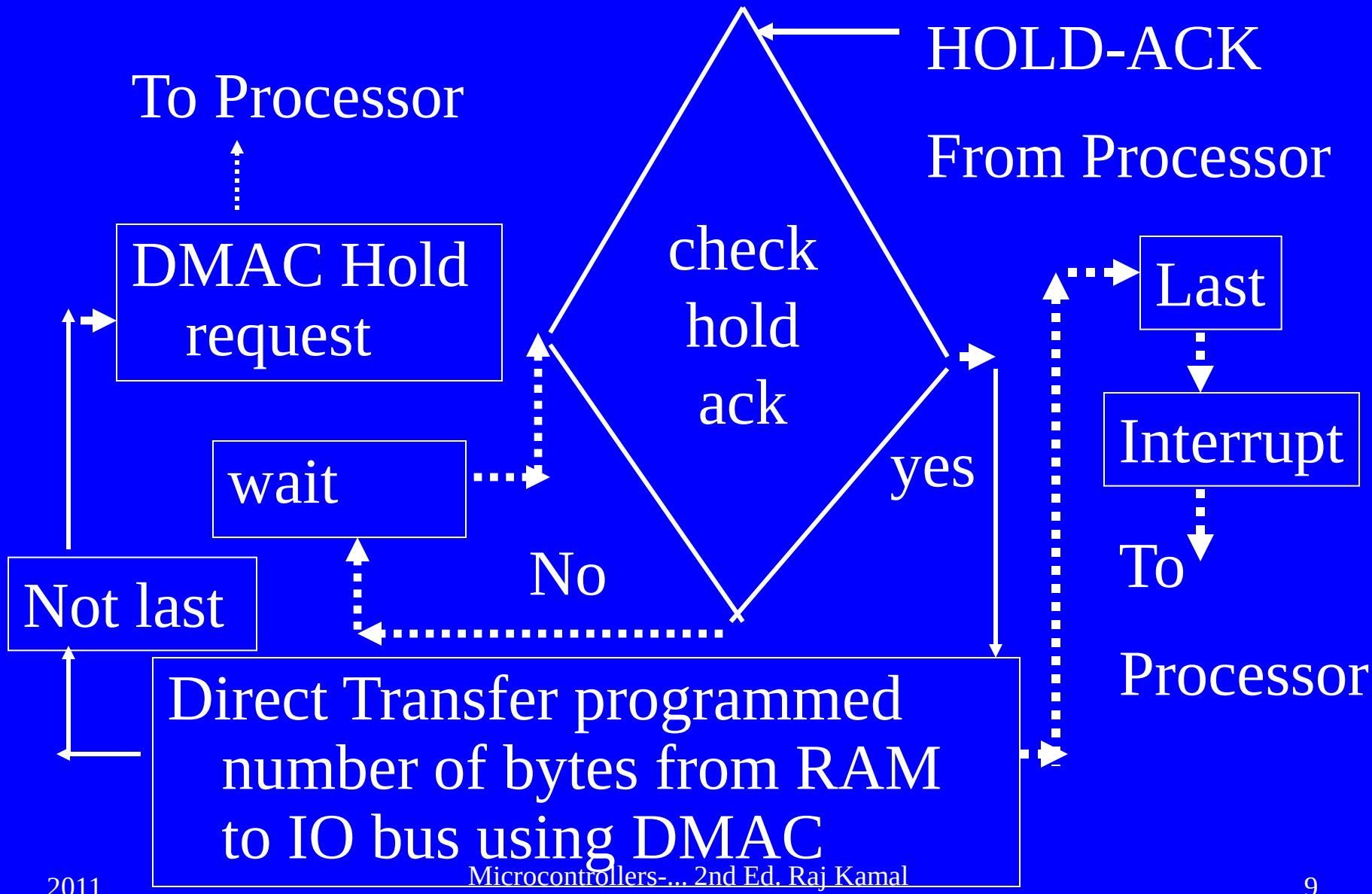
Direct Memory Access Control (Peripheral Transactions Server) IOs

- Controller or server sends hold request for processor to grant the hold-acknowledgement for the access to address and data buses, IORD, IOWR, MEMRD, MEMWR and IO buses

Direct Memory Access Control (Peripheral Transactions Server)

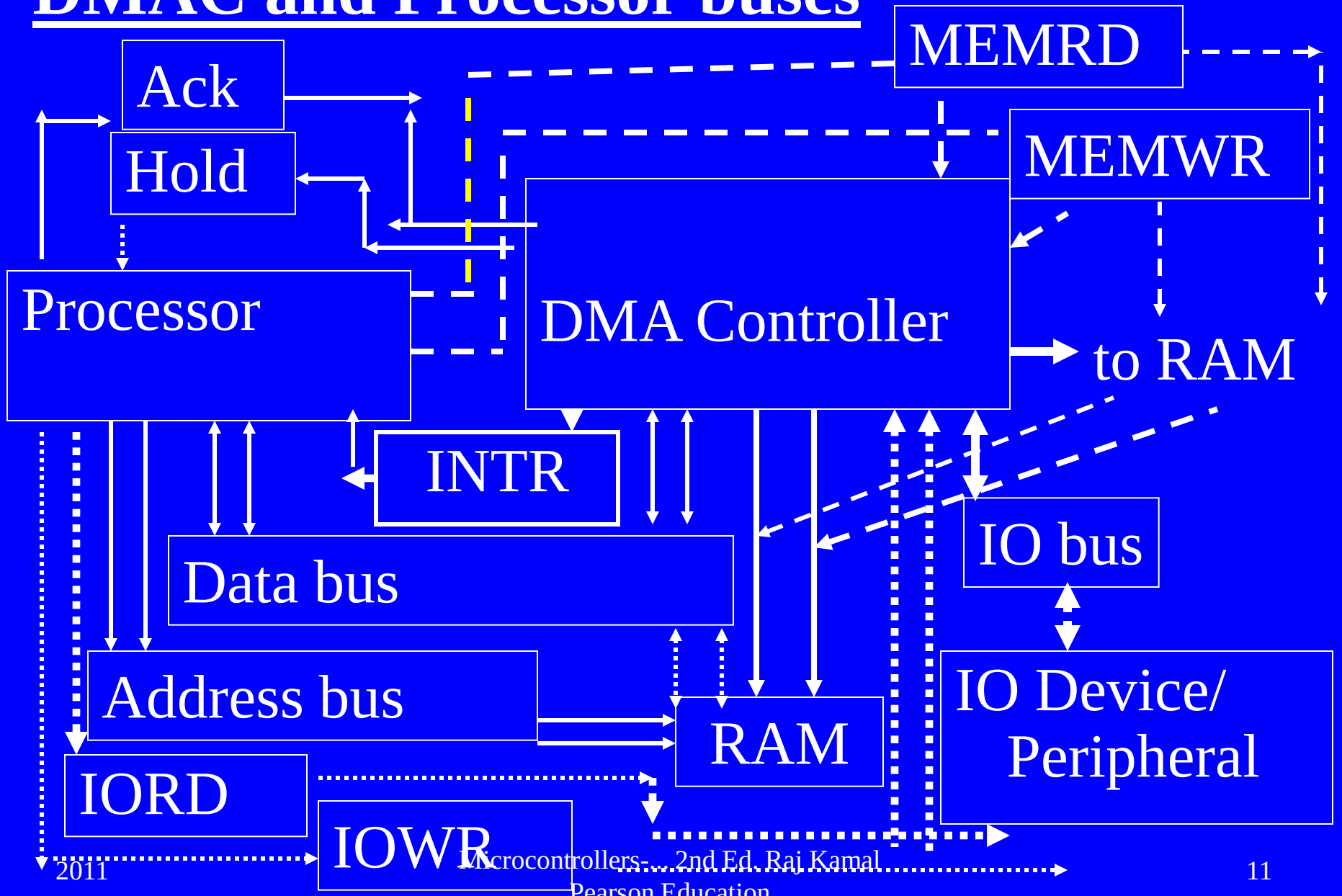
- Once programmed for address of RAM block for transfer and for data counts of IO transactions with RAM, interrupts only at the end of a block transaction or last transaction

DMA Transactions (IOs) Example

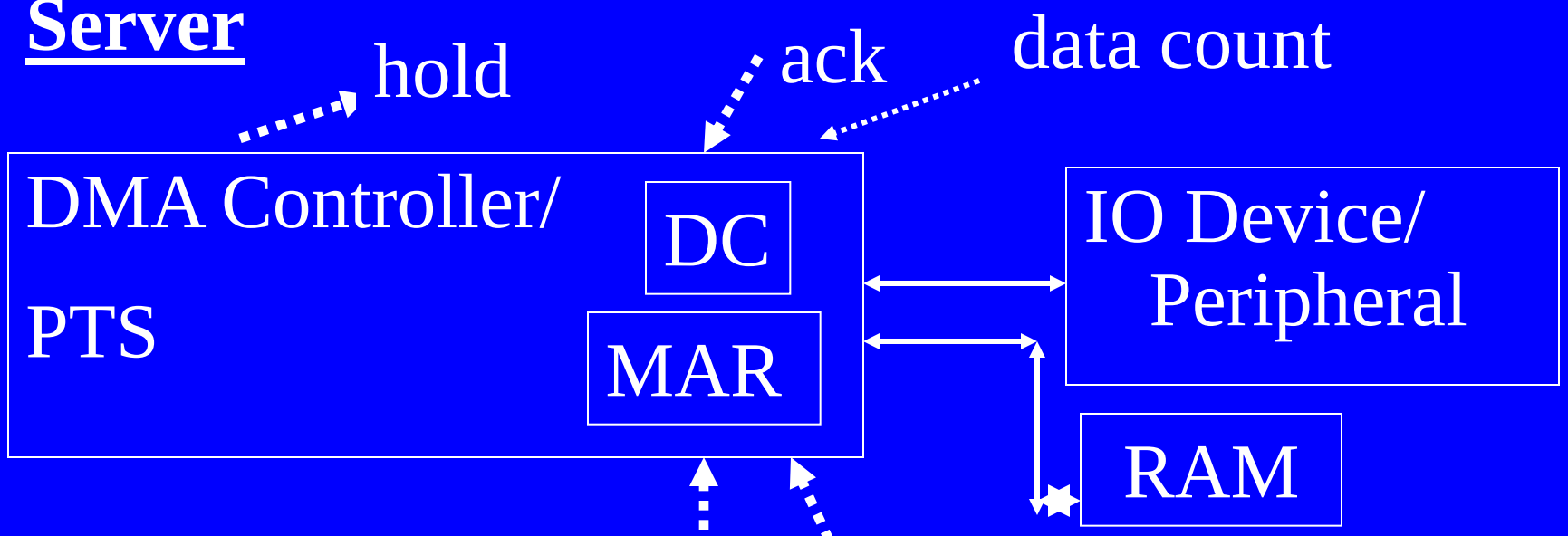


DMAC and 8257 DMAC

DMAC and Processor buses



DMAC (DMA Controller) Peripheral Transactions Server



At start, write the DMAC DC register and MAR address of RAM memory block

memory address

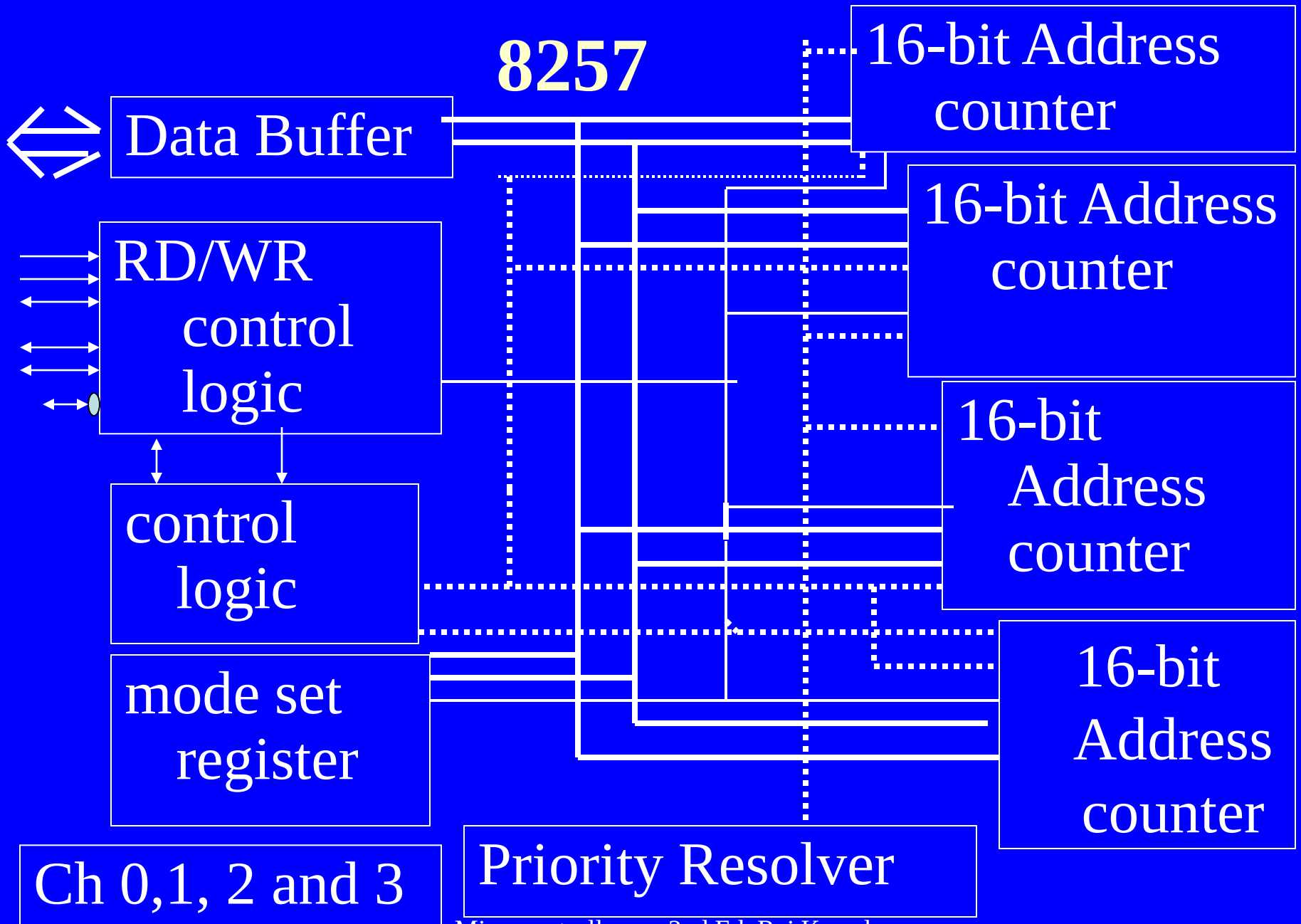
8257 Four Channel DMAC Features

- Four channels
- Priority Resolution support
- TC output and Mark output (after 126 bytes transfer) for interrupts to processor for attention

8257 Four Channel DMAC Features

- Auto-load on TC mode support for repeat transactions without reprogramming TC and MAR and mode
- TTL level inputs/outputs compatible with INTEL families

8257 Block Diagram, Pins and Interfacing


8257
16-bit Address counter
Data Buffer
16-bit Address counter
RD/WR control logic
16-bit Address counter
control logic
mode set register
16-bit Address counter
Ch 0,1, 2 and 3
Priority Resolver

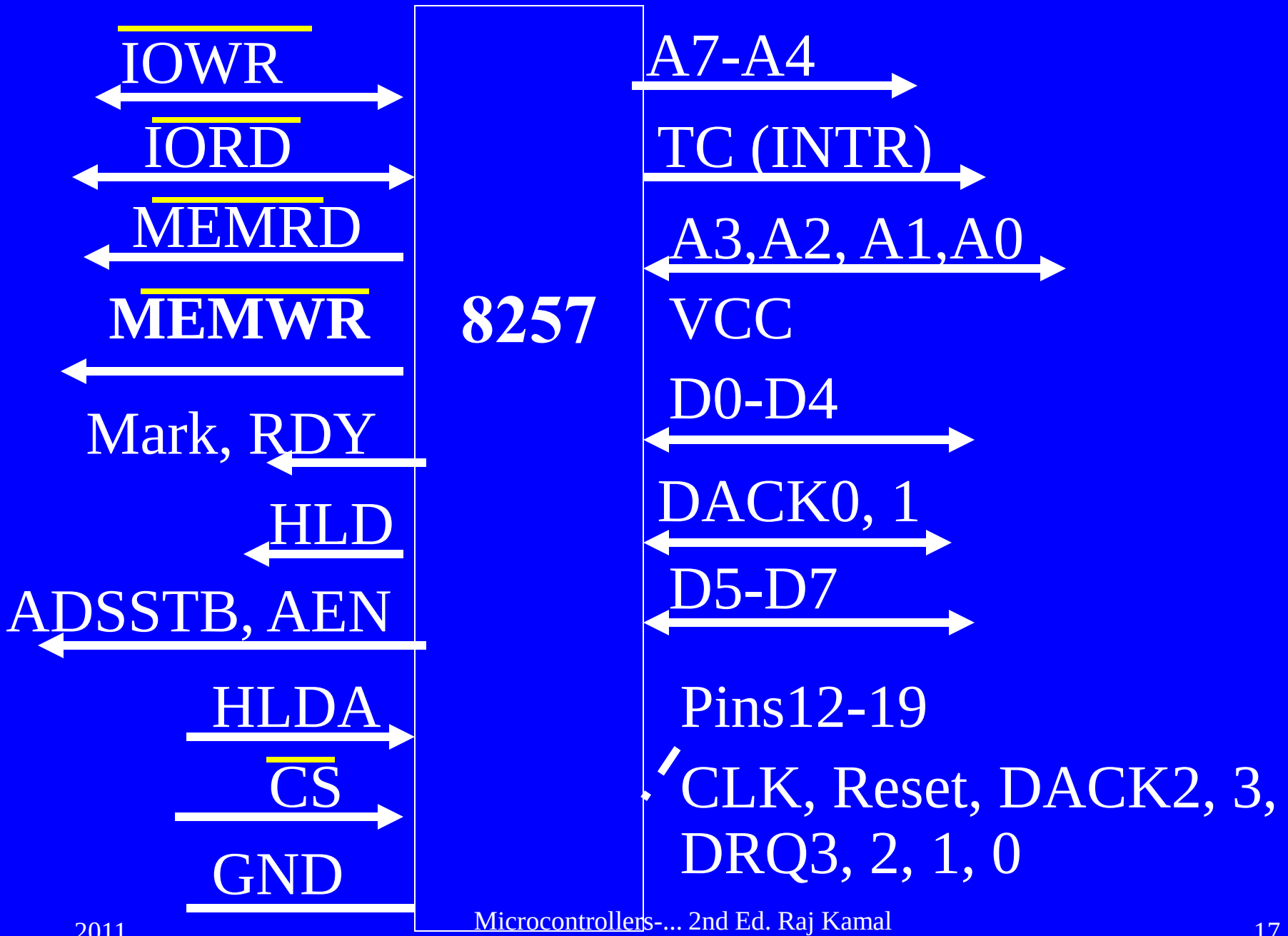

IOWR
IORD
MEMRD
MEMWR
Mark, RDY
HLD
ADSSTB, AEN
HLDA
CS
GND
8257
A7-A4
TC (INTR)
A3,A2, A1,A0
VCC
D0-D4
DACK0, 1
D5-D7
Pins12-19
CLK, Reset, DACK2, 3,
DRQ3, 2, 1, 0

Table 7.14 - Block Functions

Table 7.15 - Each Pin signals

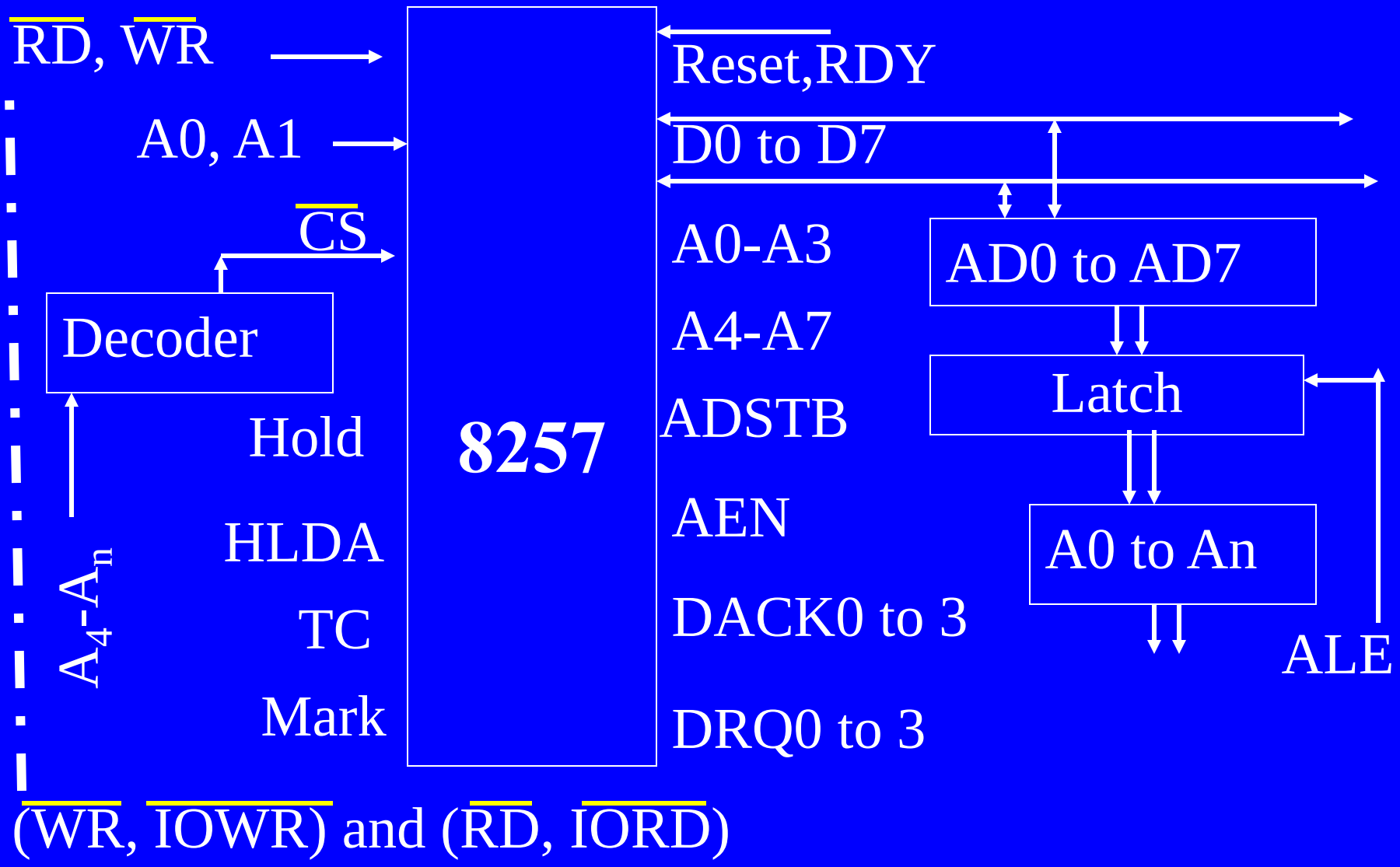

RD, WR
A0, A1
CS
Decoder
Hold
HLDA
TC
Mark
A4-An
8257
Reset,RDY
D0 to D7
A0-A3
A4-A7
ADSTB
AEN
DACK0 to 3
DRQ0 to 3
AD0 to AD7
Latch
A0 to An
ALE
(WR, IOWR) and (RD, IORD)

Figure 7.13 for details

8257 Programming

Programming the 8257 Mode and sending commands to 8257

When $\overline{CS}$ = 0,, and $\overline{IOWR}$ = 0 and A3-A2-A1-A0 = 0000, ... 1111then 8257 gets Mode/Command bytes or channel TC and DMA access MAR

Programming the 8257 Mode and sending commands to 8257

Each channel has 16 bit register with an access address (write LSB and then MSB at that address to program that)

Each channel has 16 bit register for TC register (written LSB and then MSB)

A3 = 0 for selecting a channel's address and TC registers

Programming the 8257 Mode and sending commands to 8257

0000 means ch0 MAR address, 0001TC address

0010 means ch1 MAR address, 0011TC address

0100 means ch2 MAR address, 0101TC address

0110 means ch1 MAR address, 0111TC address

Programming and reading the 8257 Mode and status

A3 = 1, $\overline{\text{IORD}}$ = 0 for selecting status register

A3 = 1 $\overline{\text{IOWR}}$ = 0 for selecting mode select register

Mode Select Register [A3A2A1A0 = 1000]

1. b0 0 disables ch0, 1 enables ch0

b1 0 disables ch1, 1 enables ch1

b2 0 disables ch2, 1 enables ch2

b3 0 disables ch3, 0 enables ch3

2. b4 = 0 disable rotating priority, 1 enable

3. b5 =0 disable extended write 1 enable extended write (next DMA repeat after TC)

Mode Select Register [A3A2A1A0 = 1000]

4. b6 0 disable terminal counter and 1 enable (stop or start DMA service)

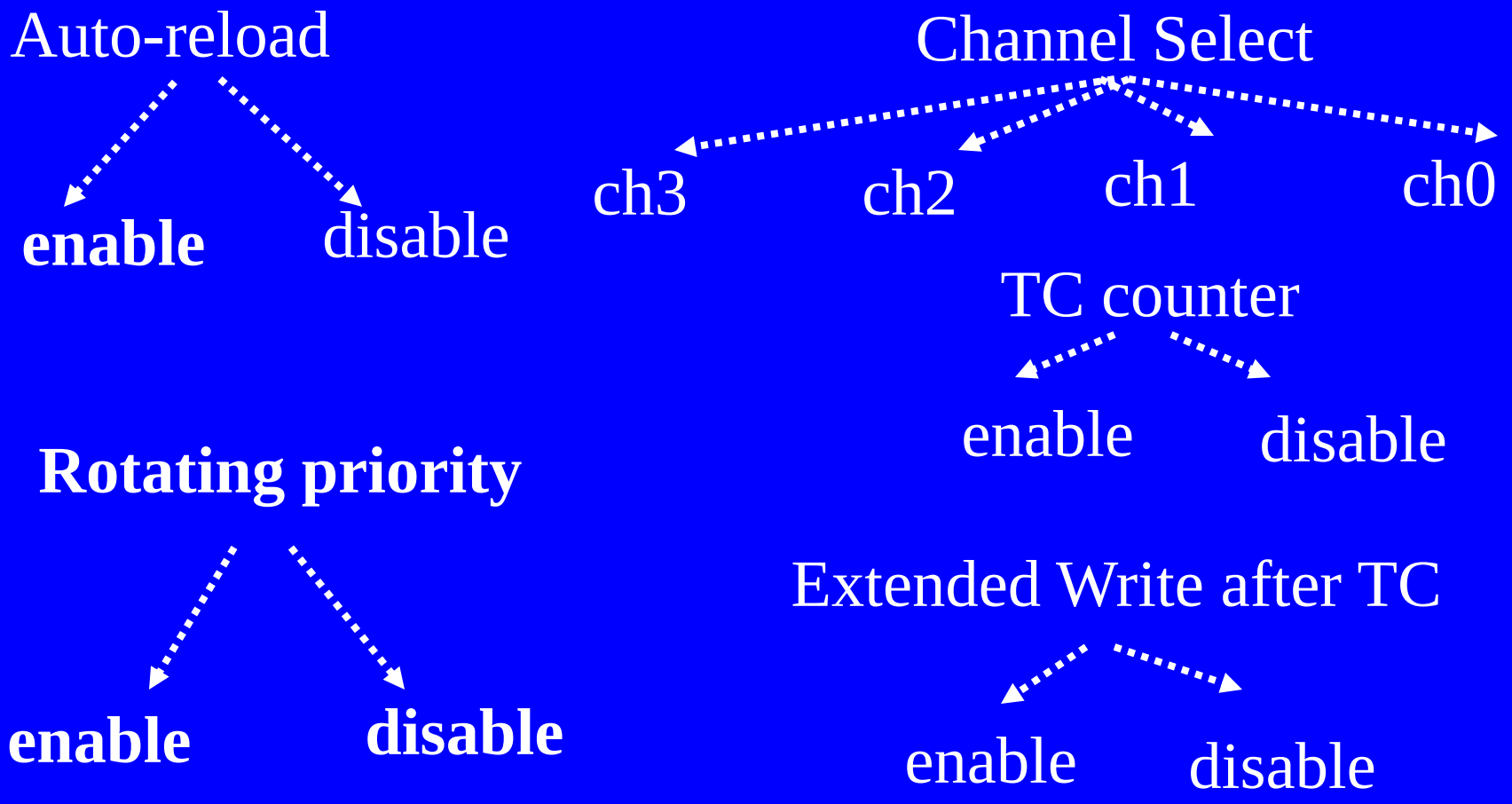
5. b7 =0 disable auto reload (of TC register and MAR of the not disabled channels 1 enable extended write (next DMA repeat after TC)

Sequential order of Bytes after reset

1. Internal registers TC and MAR of each channel

2. Mode Instruction

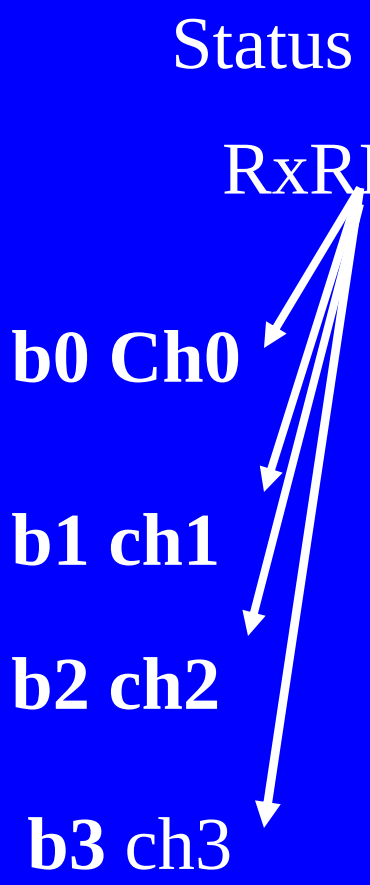
Mode Select Register



Status Byte (A3A2A1A0= 0)

When $\overline{CS}$ = 0, $\overline{IOWR}$ = 1, and $\overline{IORD}$ = 0 then 8051 reads status byte

Status Register



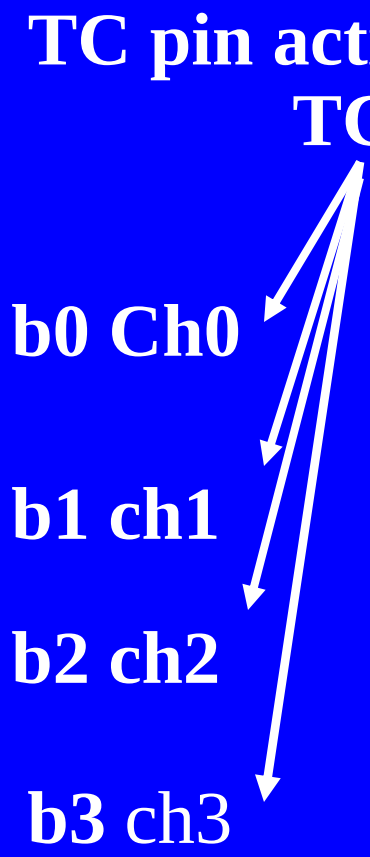
update flag

b4 update flag Auto-reload

= 1 after a reload do not write register TC and MAR when 1

b7b6b5 = 000

Status Register



Set = 1 till status register is read, auto reset to 0 when read

Refer Table 7.13for meaning of the programmed bits and status bits

Figure 7.13 - Interfacing circuit

Summary

We learnt
Three Transaction Methods

1. Programmed IOs (like 8255 port used without handshake and Intr signals)
2. Interrupt Driven IOs (like 8255 port used without handshake and Intr signals)
3. DMA Transactions using a DMAC

We learnt

4. 8257 Pins
5. 8257 Interfacing
6. 8257 Programming