Chapter 4

8051 Family Microcontrollers Instruction Set

Lesson 2

Addressing Modes

Execution of Instruction

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Instruction Execution

clock cycle (s)

STEP 1 → **Fetch opcode-bits**

STEP 2 → **Fetch bits for the operand(s)**

↓ **Time**

An addressing mode specifies, how will an operand(s) is obtained from the fetched bits before performing the operation(s) using it.

Immediate Addressing Mode

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Immediate Addressing

STEP 2 $\longrightarrow$ **Fetch bits for the operand(s)**

clock cycle (s)

$\downarrow$ **Time**

Immediate addressing mode specifies that an operand is same as the fetched bits. Operand is immediate succeeding bits after the opcode.

Example-Immediate Addressing

clock cycle (s)

For adding 08H into A register

Fetch bits for getting the operand for addition

Time

STEP 2

ADD A, #08H

Format- ADD A, #data

Sign # specifies that 08H is the immediate succeeding byte is the operand

Codes 24H, 08H in Memory-

<u>Register Addressing Mode</u>

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Register Addressing

clock cycle (s)

STEP 2 ⟶ **Fetch bits coexisting with the opcode**

↓ **Time**

Addressing mode specifies that fetch bits (coexisting with opcode of 5 bits) specify a register, operand is at that register.

Example-Register Addressing

clock cycle (s)

STEP 2 ⟶ **Use 3 bits for getting the operand register**

For transferring R1 byte into A register

Time

MOV A, R1

3 lower bits specifies that register is R1 for the operand during this operation

Code bits in Memory- 1110 1001

<u>Direct Addressing Mode</u>

Direct Addressing

clock cycle (s)

STEP 2 → **Fetch byte(s) after the opcode**

Time

Addressing mode specifies that fetch byte(s) (coexisting after the opcode of 8 bits) specify an address, the operand is at that address.

Example-Direct Addressing

clock cycle (s)

STEP 2 ⟶ **Fetch 8 bits for getting the operand address**

For transferring addressed byte into A register

Time

MOV A, 90H

8 bits directly specify the address for the operand

Code bits
E5H 90H

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Example-Direct Addressing

clock cycle (s)

STEPS 2-3 ⟶ **Fetch 16 bits for getting the operand addresses**

Time

For transferring addressed byte into another address

MOV 80H, 90H

Code bits in Memory-
85H 80H 90H

16 bits directly specify the addresses for two operands
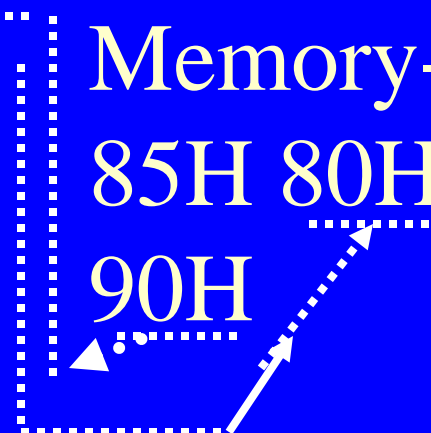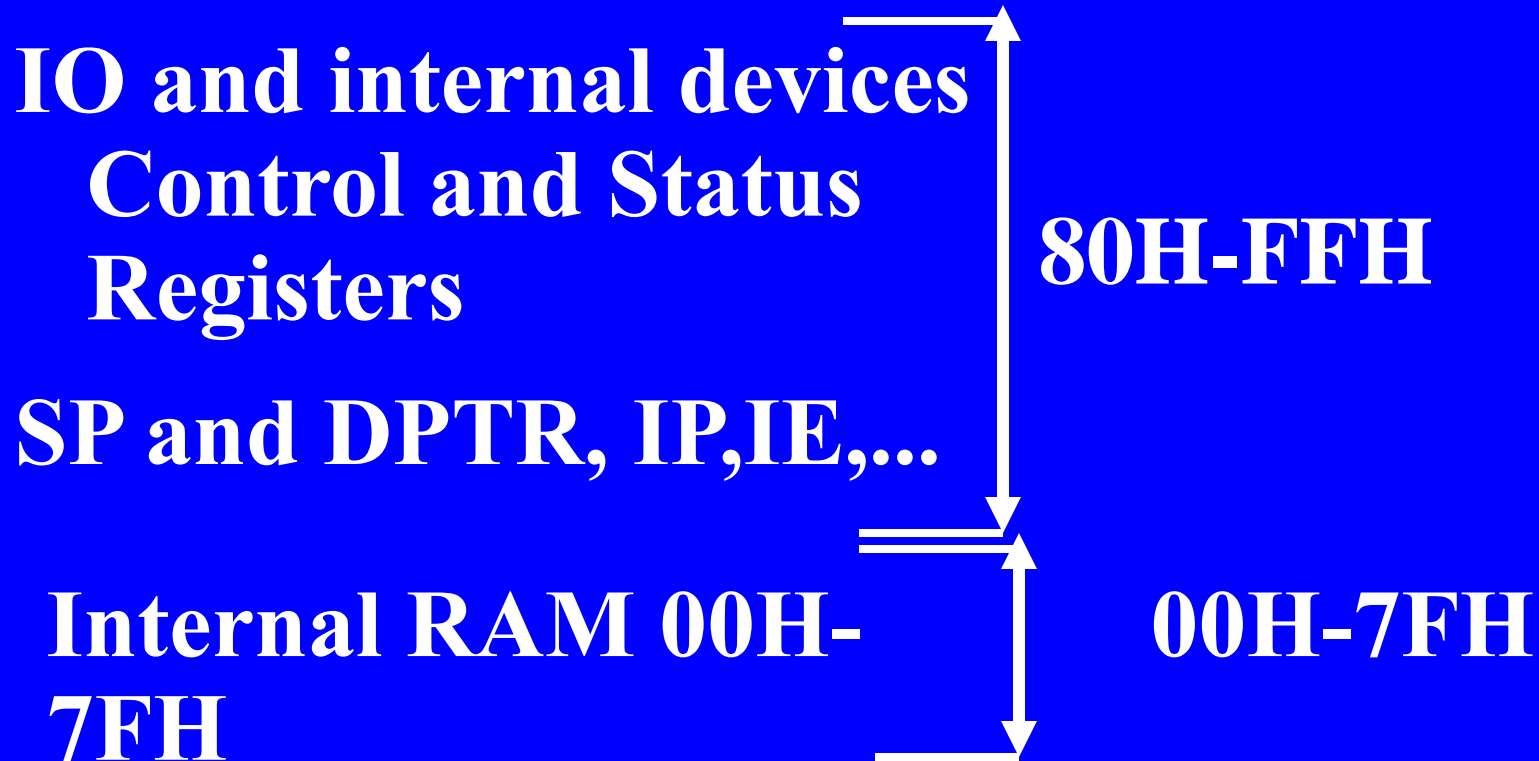
8051 family three type of instructions

using direct addressing mode

- *direct* for SFR or

- *direct* for Internal RAM in between 00H to 7FH

- *direct* for a bit at bit addressable SFR or RAM

Direct Addressing Mode

IO and internal devices Control and Status Registers

SP and DPTR, IP,IE,...

80H-FFH

Internal RAM 00H-7FH

00H-7FH

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Indirect (Index) Addressing Mode

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Internal Memory Indirect Addressing Mode

Internal Data Memory
- 128 B 8051
- 256 B 8052

Internal Program Memory (4kB)

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Always Indirect Addressing mode

Internal/External Program Memory (max. 64 kB)

External Data Memory and Ports (max 64 kB)

Indirect Addressing

clock cycle (s)

STEP 2 ⟶ **Fetch bits after the opcode**

↓ **Time**

Addressing mode specifies that fetch bits (coexisting after the opcode bits) specify a register (or address), the operand address is pointed by that
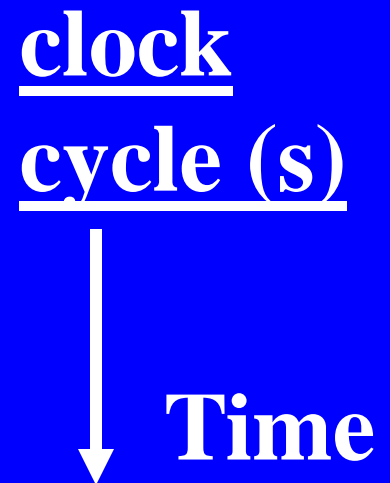
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Example-Indirect Addressing

clock cycle (s)

STEP 2

For transferring from a pointed address byte into A register

Fetch 3 bits for getting the operand address

Time

MOV A, @R1

Code bits in Memory-11100 111

3 bits specifies a register, byte at that points indirectly specify the address for the operand

Sign @ means R1 is a pointer

Example-Indirect Addressing

clock cycle (s)

STEPS 2-3
For transferring addressed code byte into A

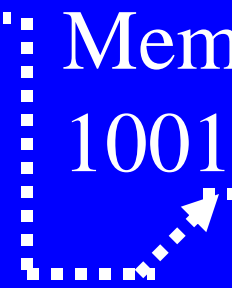**Fetch bits for getting the operand addresses**

Time

MOVC A, @A + DPTR

Code bits in Memory- 10010011

1 bit (bit4) indirectly specify DPTR,16-bits at that adds in 8-bits at A register and then 16-bits point to code at that address

Three types of instructions using indirect addressing mode

- for internal RAM 00H-FFH using R0 or R1 at a bank

- for External RAM address by R0 or R1 at a register bank at a bank

- for code memory address using PC or DPTR along with A register

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Indirect Addressing

1. Only indirect addressing in 8051 instruction for a byte in external data memory

2. Only indirect addressing in 8051 instruction for a code in internal/external program memory

3. Only indirect addressing in 8052 instruction Internal RAM between 80H-FFH

No Indirect Addressing

For 8051 instruction for an SFR

Summary

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We learnt

8051 family addressing modes

- immediate

- register

- direct for SFR

- direct for internal RAM in between 00H to 7FH

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We learnt

8051 family addressing modes

- Indirect internal RAM using R0 or R1 at a bank

- Indirect External RAM address by R0 or R1 at a register bank at a bank

- Indirect code memory address using PC or DPTR along with A register

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