

# Chapter 3

## 8051/8031 Family Architecture

## **Lesson 07**

# **Interrupts Handling**

# Interrupt ISR Start and Return

**Priority**

→ **Default Assignments**

**Push**

→ **PCH, PCH on to stack**

**Pre  
emption**

→ **Yes, in between preemption by  
higher priority interrupt if not  
masked**

# Interrupt ISR Return

**Priority** → **Default Assignments**

**Pop** → **PCH, PCH from stack**

# Interrupts Defaults Priority

High

INT0

INT0 pin interrupt

T0

T0OVF interrupt

INT1

INT0 pin interrupt

T1

T1OVF interrupt

RI and TI

RI and then Tx

T2

T2EX pin-ve edge

SI Synch  
mode

capture/reload interrupt

Synchronous Serial Device mode  
interrupt

Low

- **Enabling (unmasking) and disabling (masking) interrupts- by IE SFR bits setting and resetting**
  
- **Assigning higher 1 or lower priority 0 by overriding the default priorities = by IP SFR bits setting and resetting**

# Interrupt Masks

**Primary  
Mask**



**By resetting EA at IE.7 Bit  
address AFH masks all  
interrupts**

**Secondary  
Masks**



**By resetting E bits at  
IE.6=IE.0 Bit addresses  
AE=A0H masks the  
respective interrupts**

# IE Interrupt masks

Primary mask bit  
Enable all

IE.7 IE.6 IE.5 IE.4 IE.3 IE.2 IE.1 IE.0

EA - ET2 ES ET1 EX1 ET0 EX0

# IP interrupt Priority

IP.7 IP.6 IP.7 IP.6 IP.7 IP.6 IP.7 IP.6

- - PT2 PS PT1 PX1 PT0 PX0



**EA**

**Enable all**

**ET2**

**Enable T2**

**ES**

**Enable SI**

**ET1**

**Enable T1**

**EX1**

**Enable INT1**

**ET0**

**Enable T0**

**EX0**

**Enable INT0**

**PT2**

**Priority T2**

**PS**

**Priority SI**

**PT1**

**Priority T1**

**PX1**

**Priority INT1**

**PT0**

**Priority T0**

**PX0**

**Priority INT0**

**Interrupt enable  
bits**

**Priority Set/Reset  
bits**

# Flags for interrupts

**Identification flag at SCON,  
RI, TI at SCON.0 and .1**

**AT TCON    TF1 at SCON.7  
            TF0 at SCON.5**

**Identification flag at  
T2CON- TF2 and EXF2**

# Interrupt Vektored ISRs

Address

**0003H-0AH Timers 1 and 2**

⋮

**0053H-5AH Synch mode SI**

# ISRs addresses are as per Defaults Priority

High priority

Assigned ISR Code addresses

INT0

0003-000AH

T0

000B-0012H

INT1

0013-001AH

T1

001B-0022H

RI and TI

0023-002AH

T2

002B- onwards, before 0053H

SI Synch  
mode

0053H onwards

Low priority

2011

# Summary

# We learnt

- Interrupt System- Masking, Priorities, Vector ISR addresses