Chapter 3

8051/8031 Family Architecture

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Lesson 05

Watchdog Timer

Philips P83C528- 8051with WDT

Watchdog timer forces system reset to save from system stuck up state (hang state) during running

Philips P83C528- 8051with WDT

Timeout period 1.66 μs × 2^{14} for 16 MHz XTAL

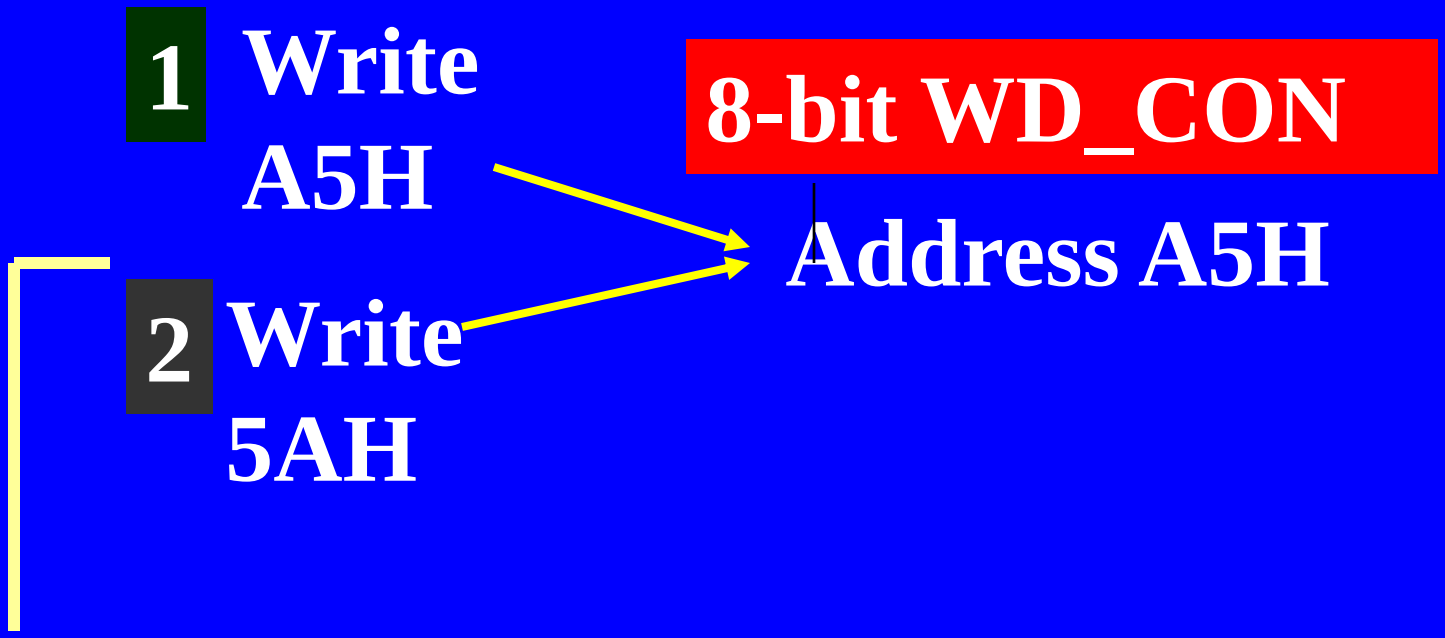
Philips P83C528- 8051with WDT

WDT starts by writing two bytes at a 16-bit address 0AH common to both bytes

Philips P83C528- 8051with WDT

Rewriting before a timeout extends the period by next cycle

Watchdog Timer control SFR



To enable writing of T3 and start WDT action, write WD_CON in sequences 1 and 2

Watchdog Timer SFR T3 in 80x96

Can be written *x* only if WD_CON written a sequence of bytes

WDT timeout Reset, PC 2080H as on power-up

Time out period = (256 − *x*)

2^{11} μs for 12 MHz XTAL

Summary

We learnt

- Watchdog Timer Use