Chapter 3

8051/8031 Family Architecture

Lesson 4

T1 Timer/Counter

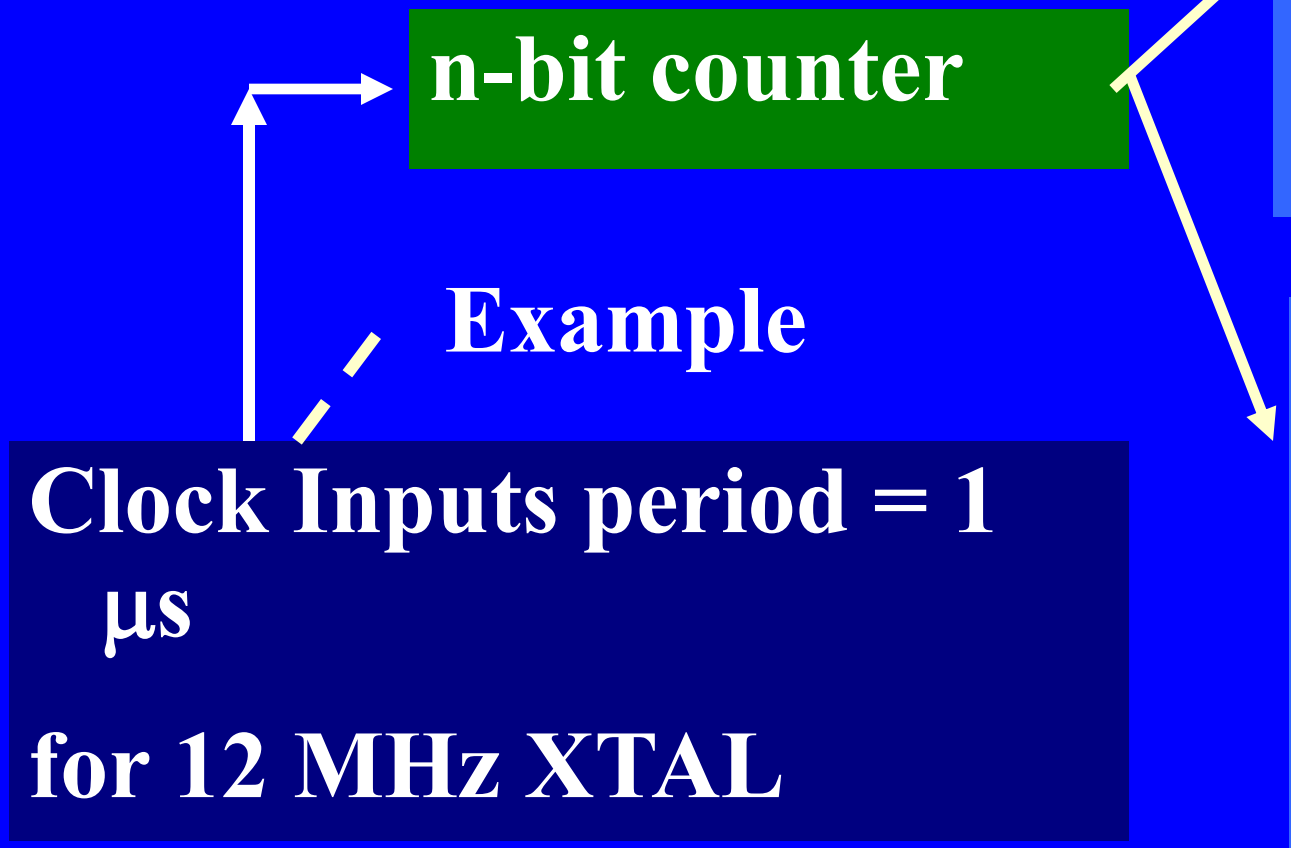
T0 Timer Counter

T2 Timer Counter (8052)

A Timer

Timer— a counter getting constant interval periodic inputs from a clock source

A timer Example



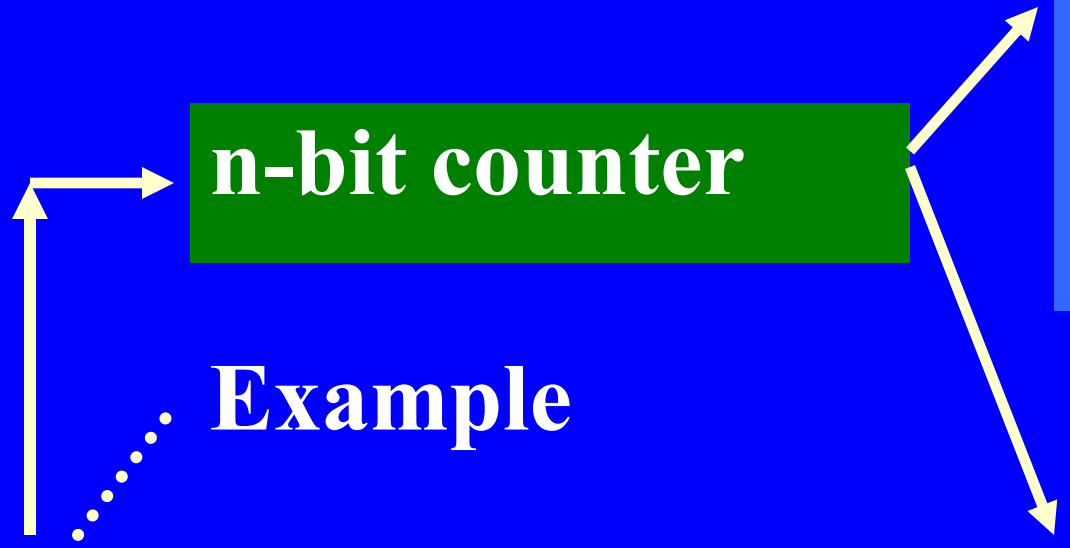
Timer overflow interrupt if not masked, then an ISR executes

Overflows after 2^n clock inputs if initial count bits all 0s.

A Counter

Counter— a timer getting irregular interval inputs from the events at a source

A Counter Example



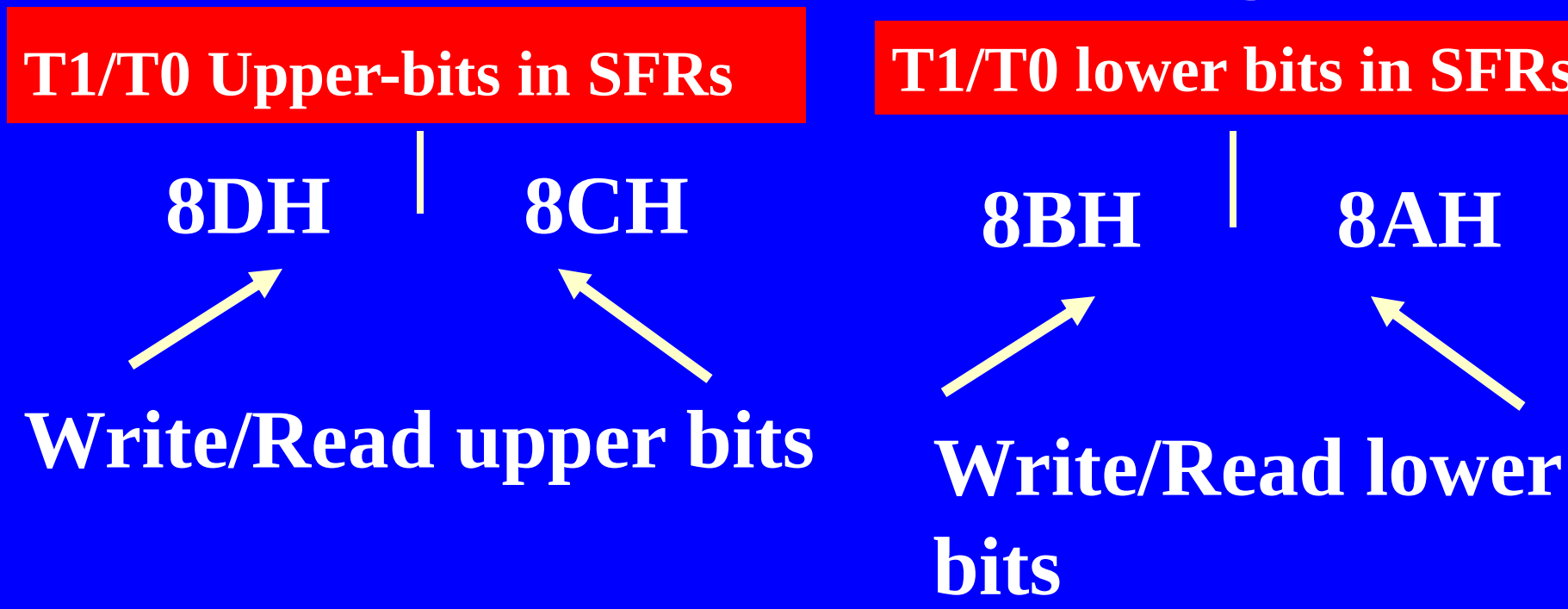
Counter overflow interrupt if not masked, then an ISR executes

Overflows after 2^n count inputs if initial count bits set = all 0s.

8051/8052 Timing/Counting Devices – T1 and T0 and T2

Timers T1 and T0 and overflows, masking and priorities of their interrupts

Timer-Counter T1/T0 SFRs Register



Overflow transition to all bits = 0s from all 1s

TF1 and *TF0* bit at TCON.7 and TCON.5 and the TF resets on an ISR start

T1/T0 Timer/Counter

Features: Stop, Reload, Internal clocking and External event-inputs

ET1 at IE.3 = 1 in IE SFR enables T1 interrupt.

ET0 at IE.1 = 1 enables T0 interrupt.

T1/T0 can gets inputs from external inputs.

T1/T0 can be externally gated to run

T1/T0 can be stopped, Can be written for load. Can be read on instruction for move, store or add or other executes.

Inputs period = 1 μs for 12 MHz XTAL

when internal timer clocking mode is used.

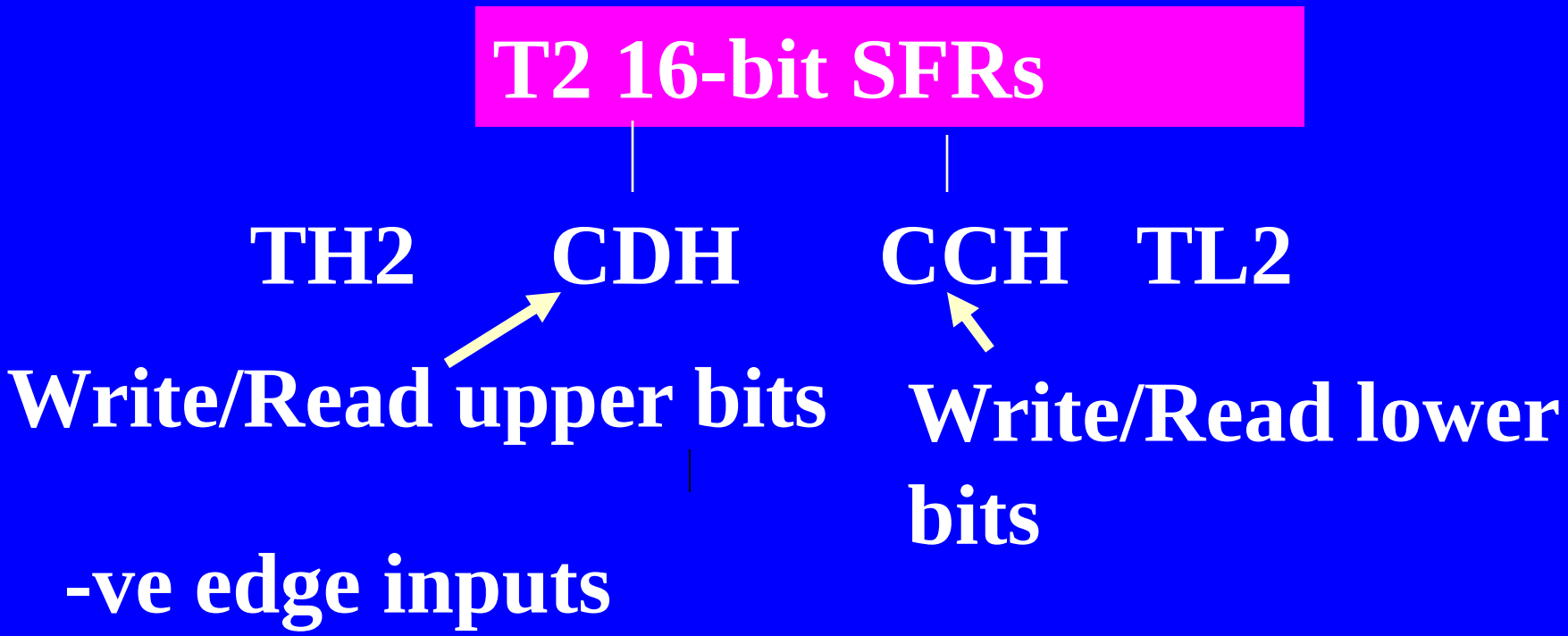
1. T1/T0 Increments by -ve edges when TR1/TR0 written = 1 at TCON.6/TCON.4, respectively

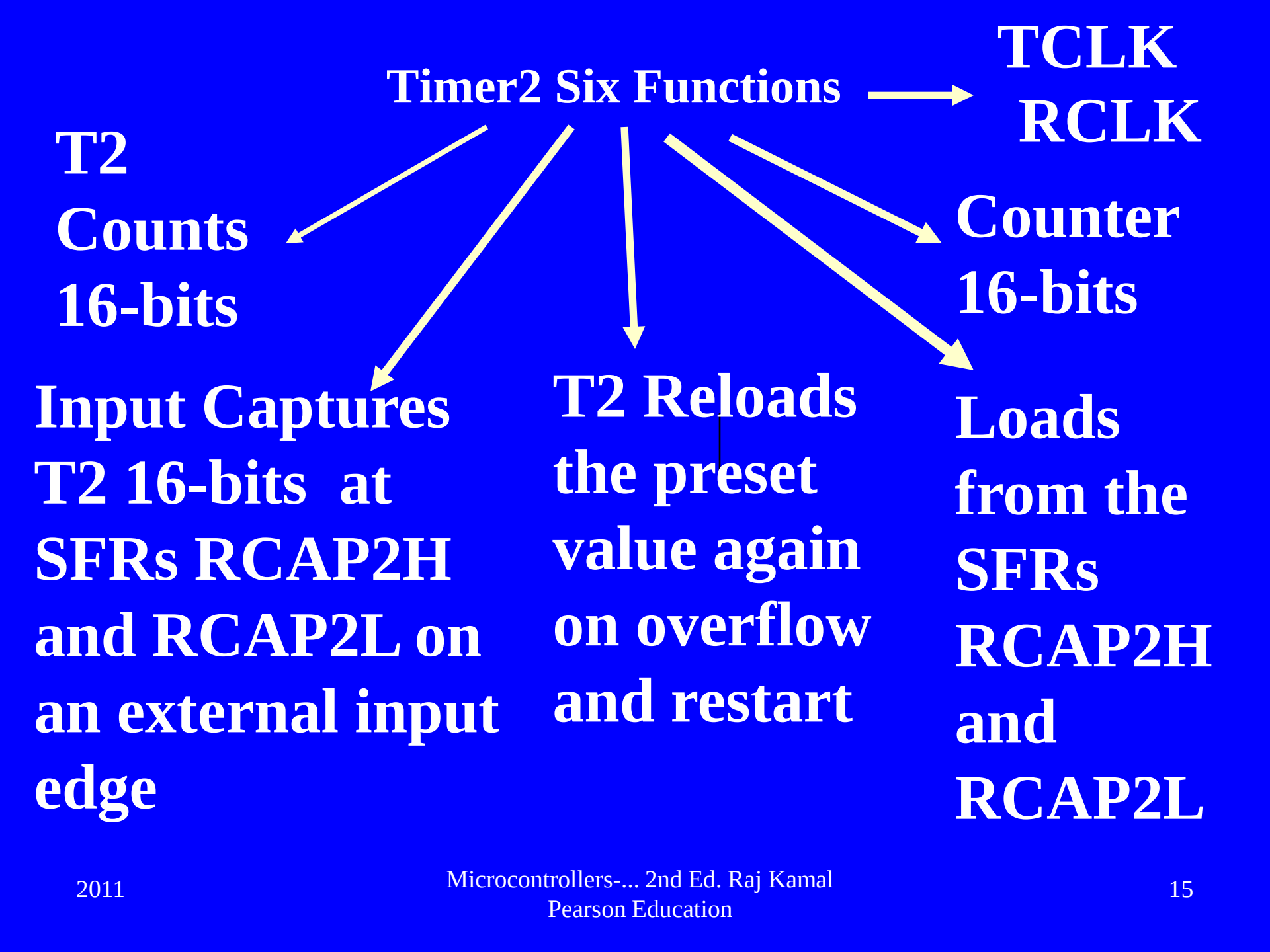
2. Event counter T1 and T0 gets count inputs from T1 and T0 pin (P3.5 and P3.4) or from the system Internal clock

3. PT1 at IP.3 = 1 enables priority high for T1 interrupt. PT0 at IP.1 = 1 enables priority high for T0 interrupt.

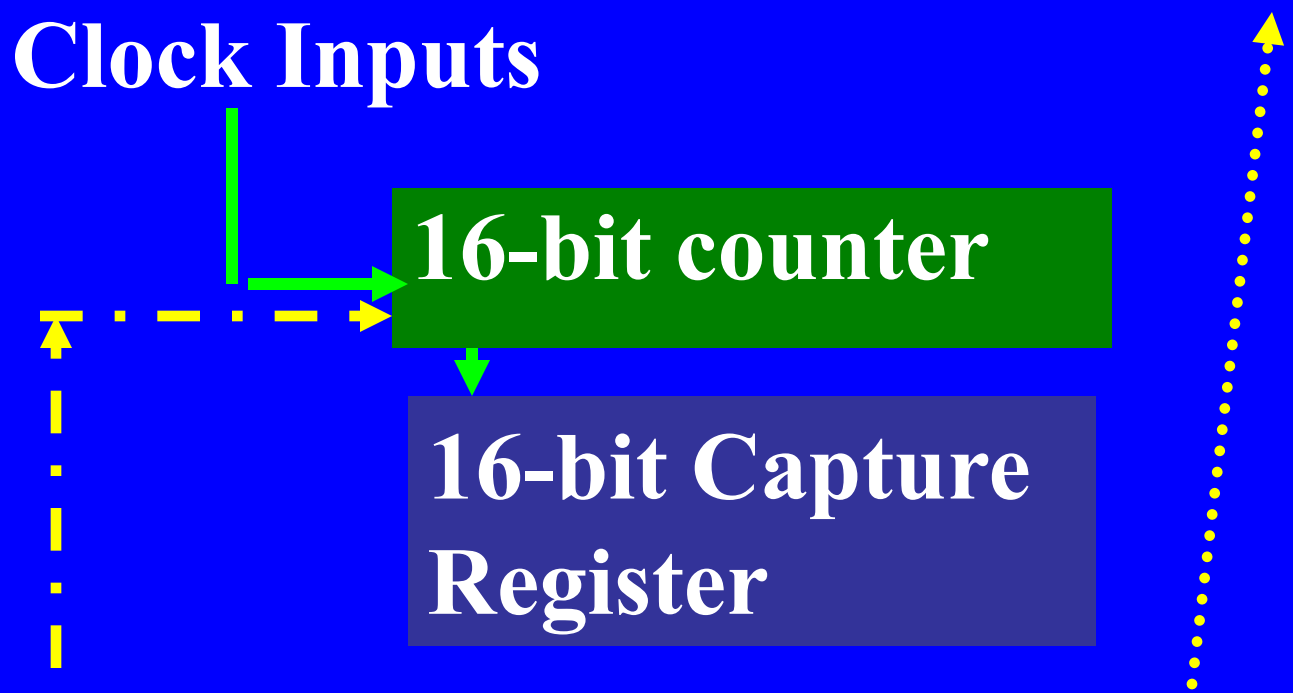
T2 (8052)

Timer-Count T2 SFRs




Timer2 Six Functions
TCLK
RCLK
T2
Counts
16-bits
Counter
16-bits
Input Captures
T2 16-bits at
SFRs RCAP2H
and RCAP2L on
an external input
edge
T2 Reloads
the preset
value again
on overflow
and restart
Loads
from the
SFRs
RCAP2H
and
RCAP2L

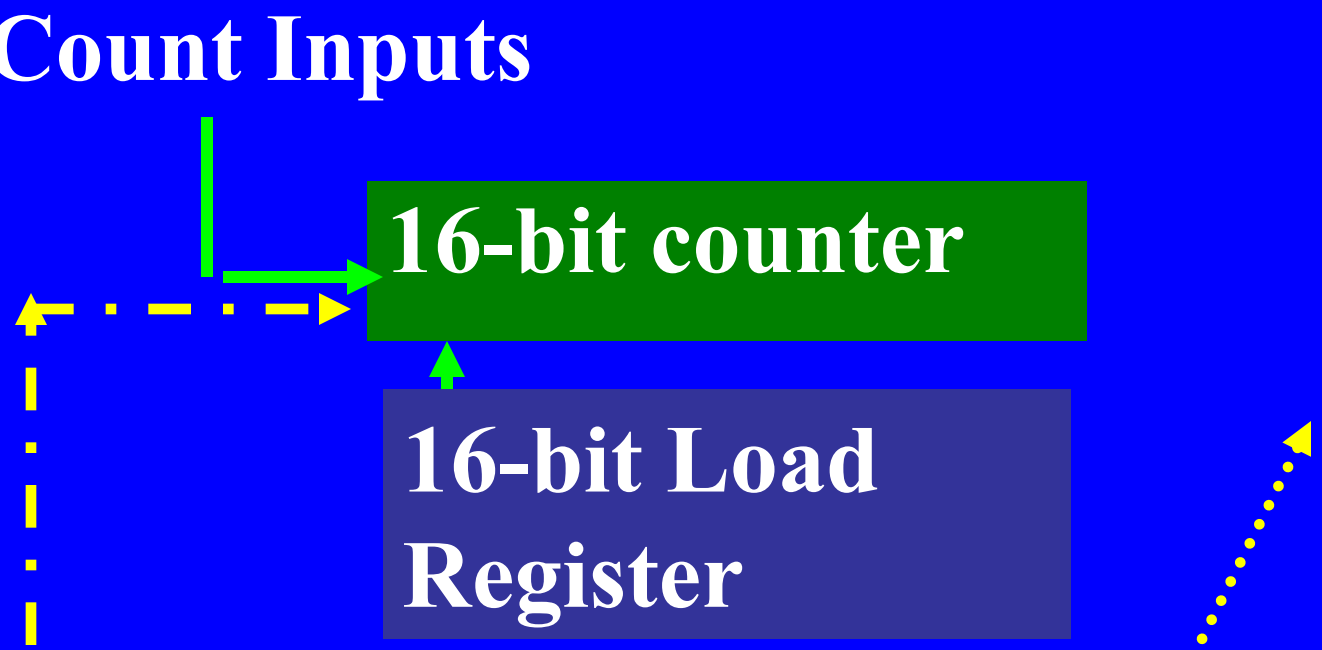
An Input Capture of Timer



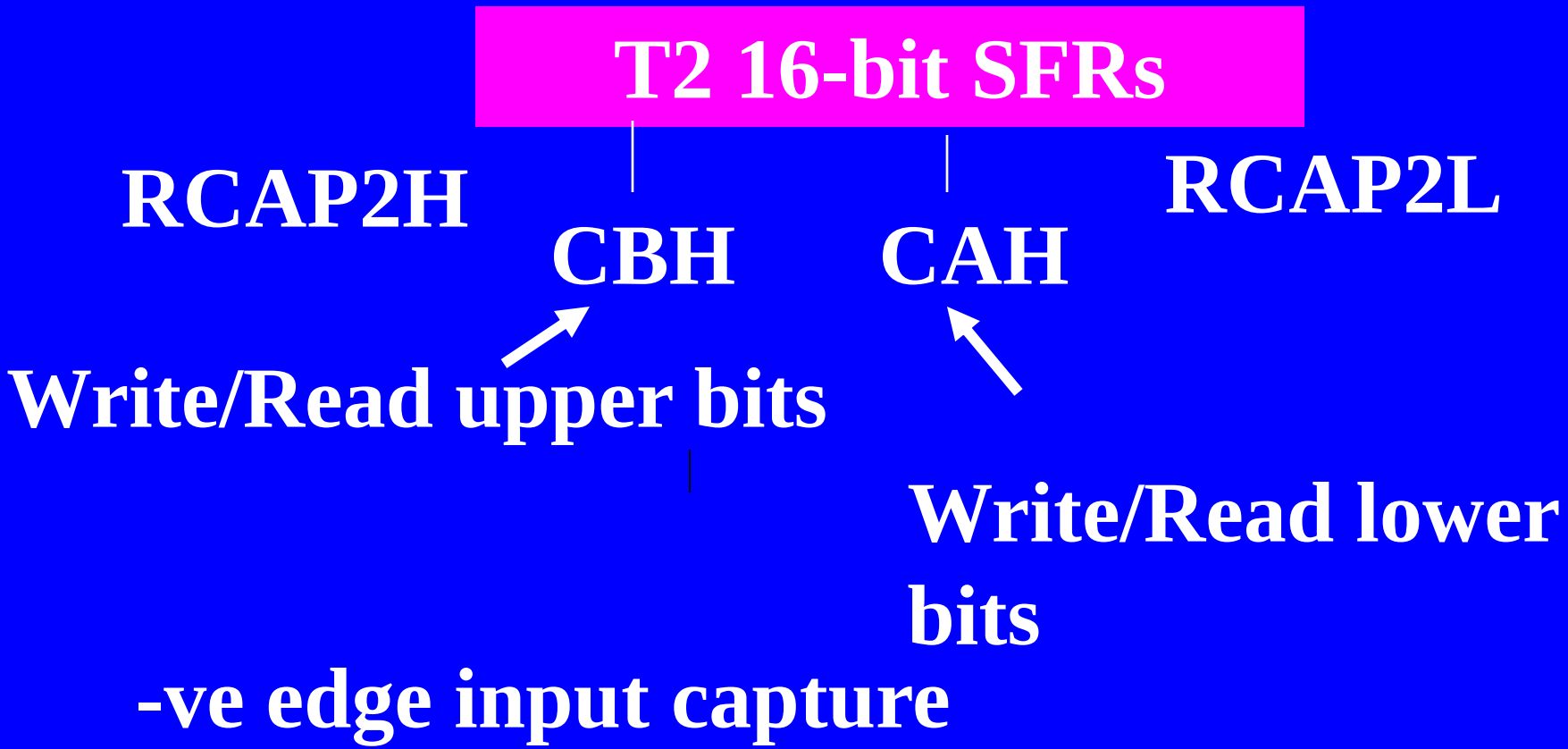
Timer capture interrupt if not masked, then an ISR executes

An edge forcing copying of the counter reading into Capture Register if capture enabled

A Reload of Counter on an input



Reload-Capture T2 SFRs



Modes 0, 1, 2 and 3 8051 timers

Using TimerT1

Write 4 bits for **mode/control in 8-bit TMOD for the for the timerT1**

Using TimerT0

Write 4 bits for mode/control bits in 8-bit TMOD for the timerT0

Timer-counter T1

16- bits TH1-TL1 no pre-scaling

8- bits TH1

Mode 0 **Mode 1** **Mode 2**

8- bits TL1

TH1 counts after pre scaling by factor of 32

TL1 counts the count/clock inputs. TL1 loads counts from TH1 on start and on each overflow

Pre-scaling means the counts or clock-inputs divide by 32 before TH1 gets the inputs.TL1 does prescaling

Timer-counter T1

Mode 3 case of T0

- T1 overflow interrupts stopped (frozen) as TH0 functions as 8-bit timer-counter overflows in place ofT1
- TL0 functions as 8-bit timer-counter T0 and overflows

.T1 can continue to generate TCLK and RCLK for the serial interface

Timer-counter T0

16- bits TH0-TL0 no pre-scaling

8- bits TH0

Mode 0 **Mode 1** **Mode 2**

8- bits TL0

TH0 counts after pre scaling by factor of 32

Pre-scaling means the counts or clock-inputs divide by 32 before TH0 gets the inputs.TL0 does prescaling

TL0 counts the count/clock inputs. TL0 loads counts from TH0 on start and on each overflow

Timer-counter T0

Mode 3 case of T0

- TH0 functions as 8-bit timer-counter overflows in place ofT1 and uses TF1 and TR1
- TL0 functions as 8-bit timer-counter T0 and overflows and uses TF0 and TR0

$\overline{GT}$1 bit = 1 disables T1 gate1 pin input
$\overline{GT}$1, T1 runs only by TR1 bit set = 1.When bit = 0, T1 run enables after gate1 pin input = 0 after the TR bit is set

$\overline{GT}$0 bit = 1 disables T0 gate0 pin input
$\overline{GT}$0, T0 runs only by TR0 bit set = 1.When bit = 0, T0 enables run after gate0 pin input = 0 after the TR bit is set

Define disable/enable T1/T0 gate input

Defining T1/T0 as counter or timer

C/$\overline{T1}$ bit = 1 disables internal clock inputs, T1 runs by external count-inputs at $\overline{T1}$ pin.When bit = 0, enables internal clock inputs to T1, disable T1 pin inputs

C/T0 bit = 1 disables internal clock inputs, T0 runs by external count-inputs at T0 pin.When bit = 0, enables internal clock inputs to T0, disables $\overline{T0}$ pin inputs.

Timers' control

TCON: T1-T0 Control and status SFR

Timer overflow Flags TF1-TF0 for the T1andT0 overflows

TCON.7 and TCON.5 show the flag statuses

TCON: T1-T0 Control and status SFR

Timer Run control TR1-TR0 for T1andT0 run

TCON.6 and TCON.4 control the running of T1-T0

External Interrupts ’ control

External Interrupt Enable SFR

IE0 bit = 1 at TCON.0 enable interrupt and = 0 disables at INT0 (GT0) pin

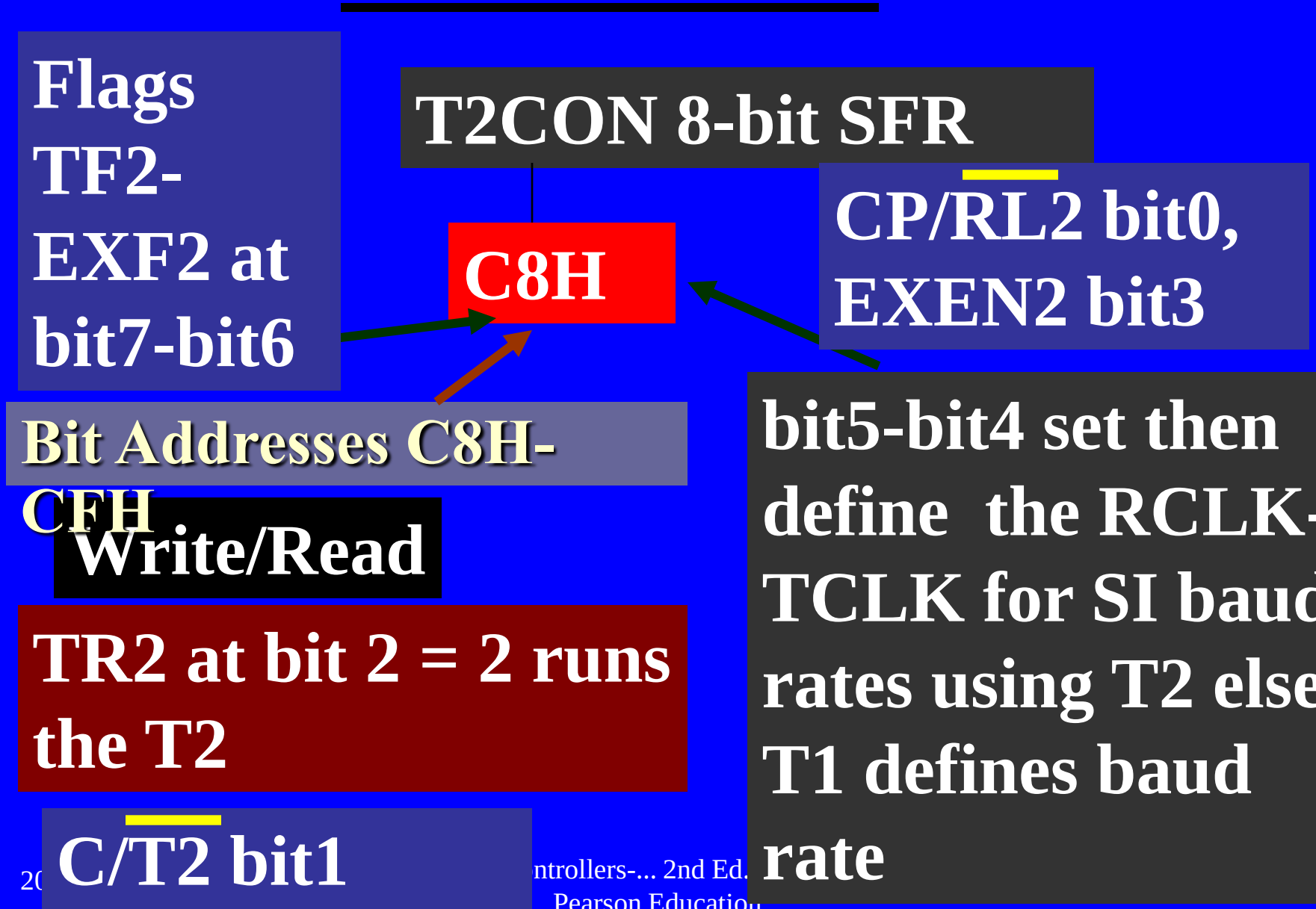
IE1 bit = 1 at TCON.3 enable -ve edge transition interrupt and = 0 enables level 0 interrupt at INT1 (GT1) pin

Enable/disable Interrupt at INT0 /INT1 pin

Defining Interrupt type at INT0/INT1 pin

IT0 bit = 1 at TCON.0 enable -ve edge transition interrupt and = 0 enables level 0 interrupt at INT0 pin

IT1 bit = 1 at TCON.2 enable -ve edge transition interrupt and = 0 enables level 0 interrupt at INT1 pin


Flags TF2-EXF2 at bit7-bit6
T2CON 8-bit SFR
C8H
CP/RL2 bit0, EXEN2 bit3
Bit Addresses C8H-CFH
Write/Read
TR2 at bit 2 = 2 runs the T2
C/T2 bit1
bit5-bit4 set then define the RCLK-TCLK for SI baud rates using T2 else T1 defines baud rate

T2 Control and status SFR

Defining T2 as counter or timer

C/$\overline{T2}$ bit = 1 at T2CON.1 disables internal clock inputs, T2runs by external count-inputs at $\overline{T2}$ pin.

When bit = 0, enables internal clock inputs to T2, disable T2 pin inputs

T2 Control and status SFR

Timer overflow Flag TF2 for T2 overflow

T2CON.7 shows the flag status

T2 Control and status SFR

EXEN at T2CON.2 enables external input capture or reload by -ve edge at P1.1 T2EX/INT2 pin

T2 Control and status SFR

Timer Capture Flag EXF2 = 1 a -ve edge at P1.1 pin forces the T2 reload from RCAP2H-RCAP2L provided EXEN control bit is 1 and when CP/RL2 (T2CON.0) = 0 (defined for reload)

Summary

We learnt

Timer DevicesT0 and T1

- T0 functions in 4 modes
- T1 functions in 3 modes

Four modes are 8-bit mode with pre-scaling by 32, 16-bit mode, 8-bit auto reload mode and two independent 8-bit timers mode

We learnt

Timers T0, T1 and T2 Actions

- T0, T1 and T2 overflows and interrupts
- T2 captures 16-bit T2 in RCAP2H-RCAP2L on a reload input
- T2 reloads 16-bit from RCAP2H-RCAP2L on a reload input
- T2 controls RCLK-TCLK in place of T1 for SI device