

# Chapter 3

## 8051/8031 Family Architecture

# Lesson 3

## **8051 MCU Devices, IO Ports and SFRs**

# Internal Devices

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Port P0

Port P2

Port P1

Port P3

T0

T1

WDT

SI

T2 in 8052

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## Internal Devices

- T0 (Timer-Counter) with four modes 0 to 3
- T1 (Timer-Counter) with four modes 0 to 3
- SI (Serial Interface) with full duplex UART or half duplex synchronous serial communication
- WDT (watchdog timer)

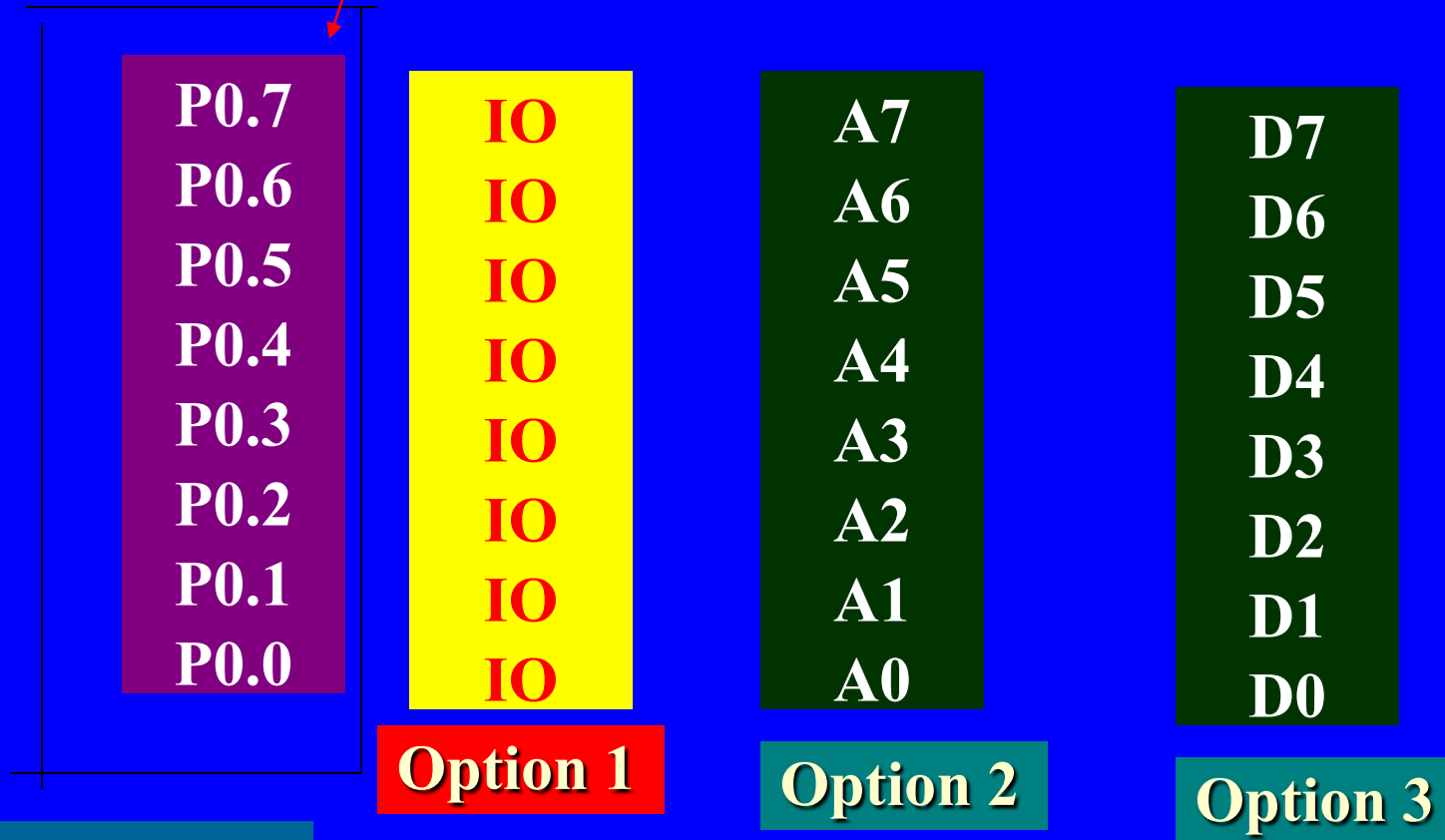
# Port SFRs

# Ports P0 Address



**Bit Addresses 80H-87H**

**Byte Address  
80H**



**Bit Addresses  
80H-87H**

# Port P0



# Ports P1 Address



**Bit Addresses 90H-97H**

# Port P1

**Byte Address**  
– 90H

P1.7	IO
P1.6	IO
P1.5	IO
P1.4	IO
P1.3	IO
P1.2	IO
P1.1	IO
P1.0	IO

**Options**

Timer T2  
8052, I2C and  
other devices  
signals

**Option 1**

**Bit Addresses 90H-97H**

# Ports P2 Address



**Bit Addresses A0H-A7H**

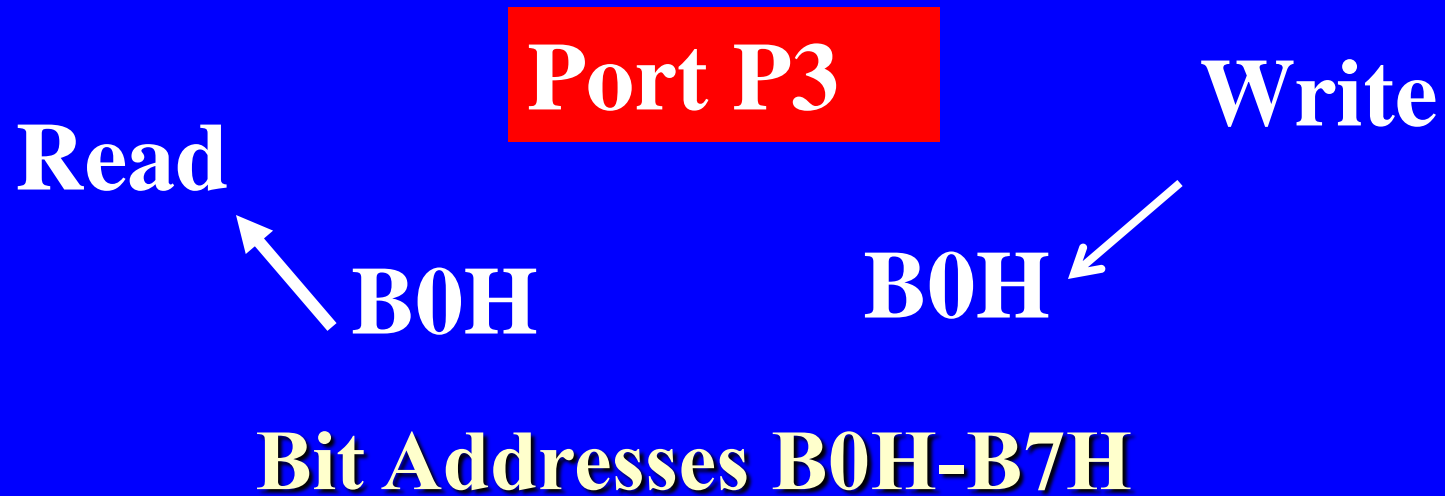
**Byte Address**  
**A0H**



**Bit Addresses**  
**A0H-A7H**

# Port P2

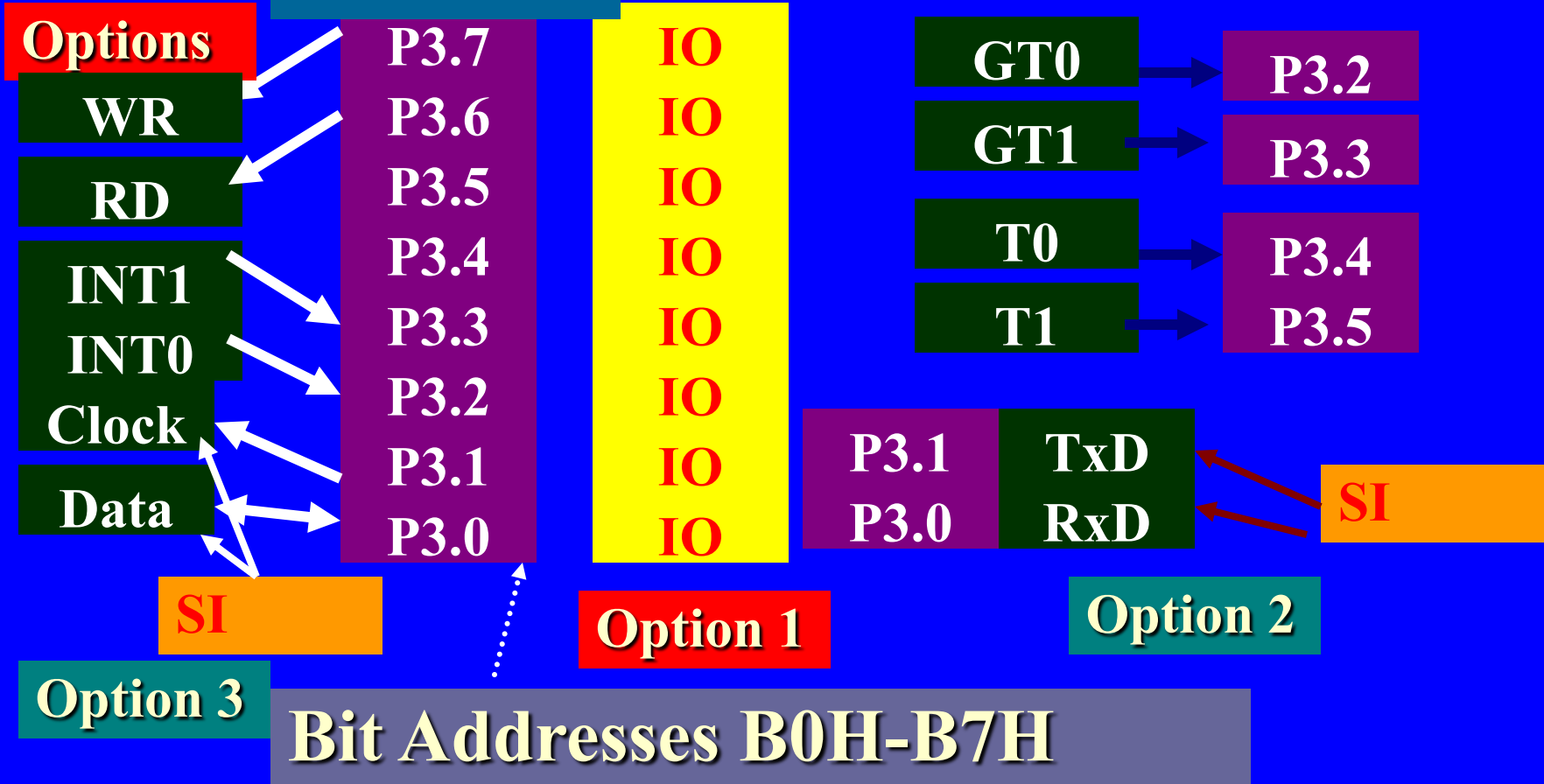
# Ports P3 Address



# Port P3

Byte Address  
– B0H

Options



# Ports P0-P1-P2-P3 in Single chip mode

- Bi-directional open drain port (needs external pull up circuit) for output
- A bit must first be written 1 then used as input

## Port P0 in Expanded mode

- P0- When used as AD0-AD7 then a weak internal pull up and functions as quasi bi-directional with a weak internal pull up- just sufficient to drive LSTTL latch for two clock periods. [Maximum 8 LSTTLs]



# Ports P2, P1 and P3 in Expanded mode

- Bi-directional quasi bi-directional with a weak internal pull up
- Maximum 4 LSTTLs at output
- 1 LSTTL input

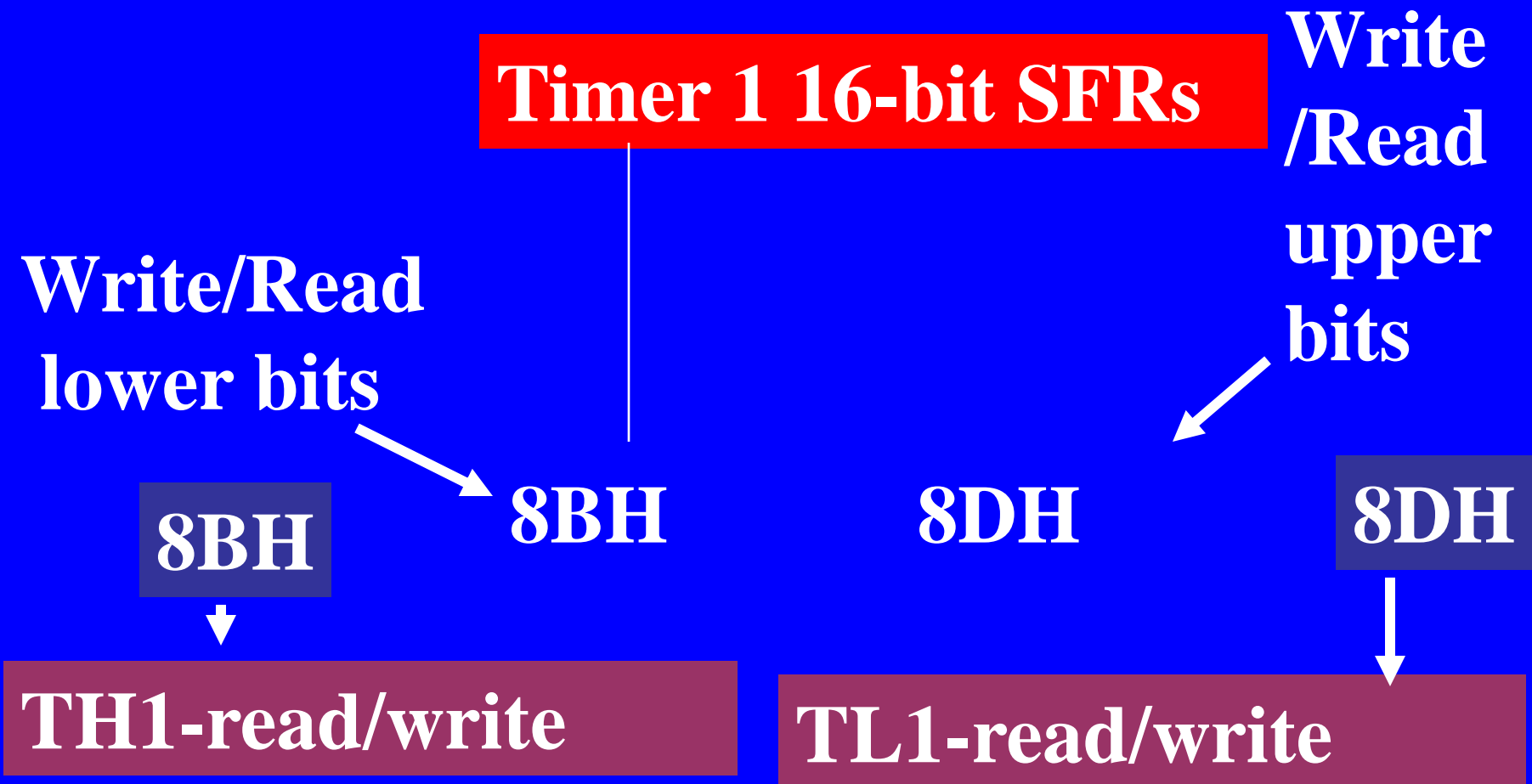
# Devices SFRs

# **IO and internal devices Control and Status/System/CPU SFRs 80H-FFH**

# T1: Timer cum Counter Device

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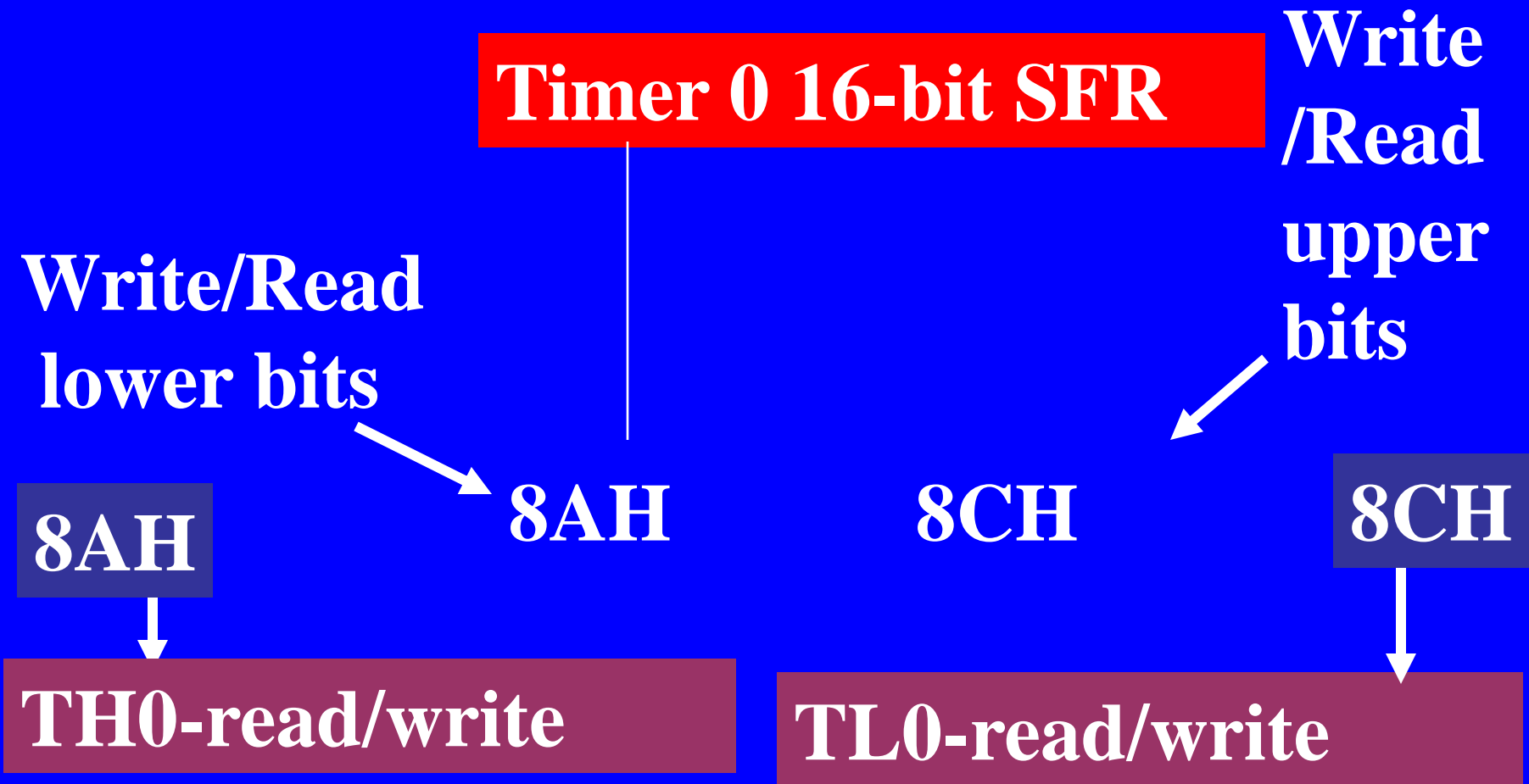
# T1 Timer-Count SFR Addresses



# **T0: Timer cum Counting Device**

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# T0Timer-Count SFR addresses



# Timer-Counter Mode control SFR Address

**TMOD 8-bit SFR**

**Write  
/Read  
upper  
4 bits**

**Write/Read  
lower 4 bits**

**89H**

**89H**

**89H**

**89H**

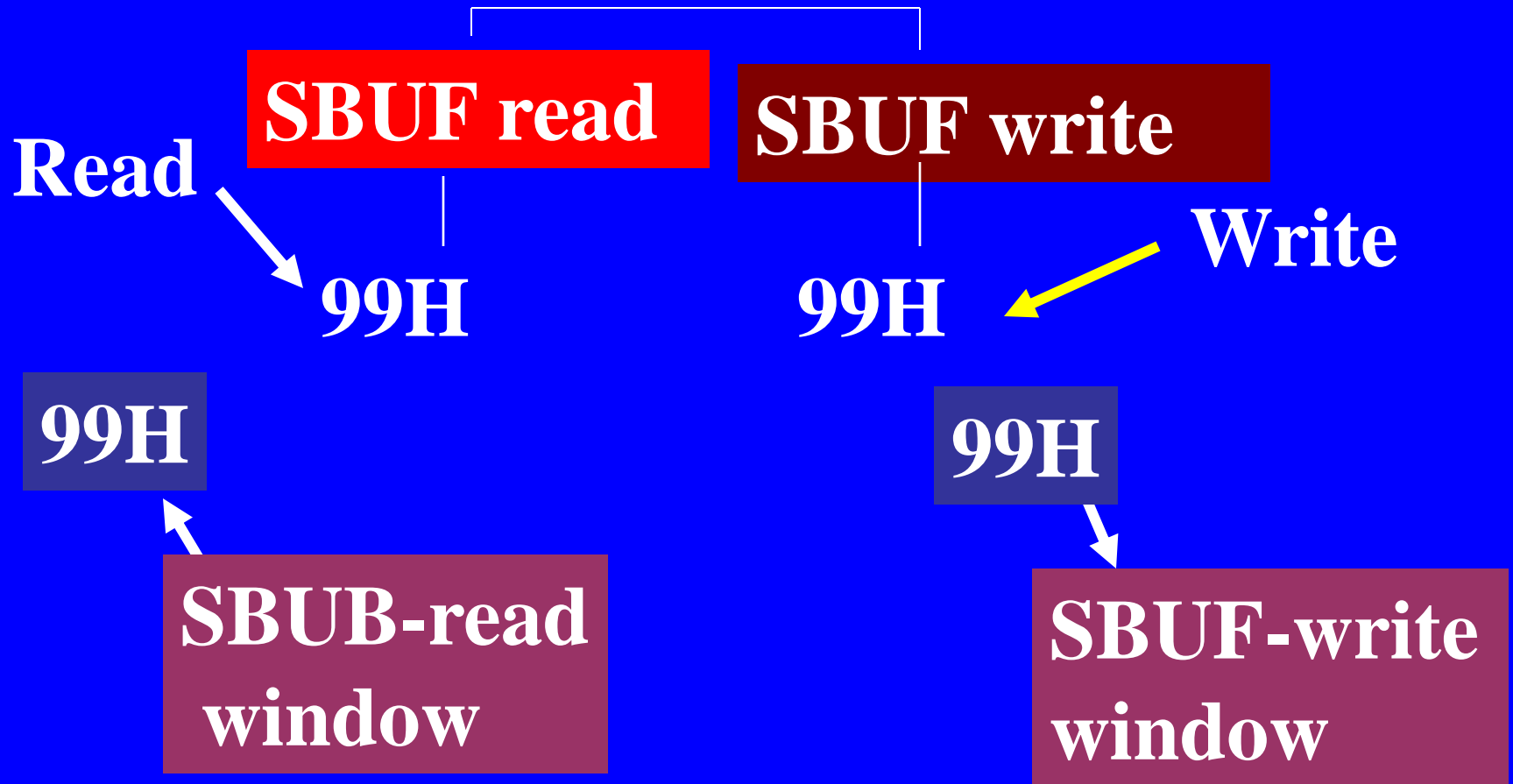
**Timer 1  
mode/control bits  
read/write**

**Timer 0  
mode/control bits -  
read/write**



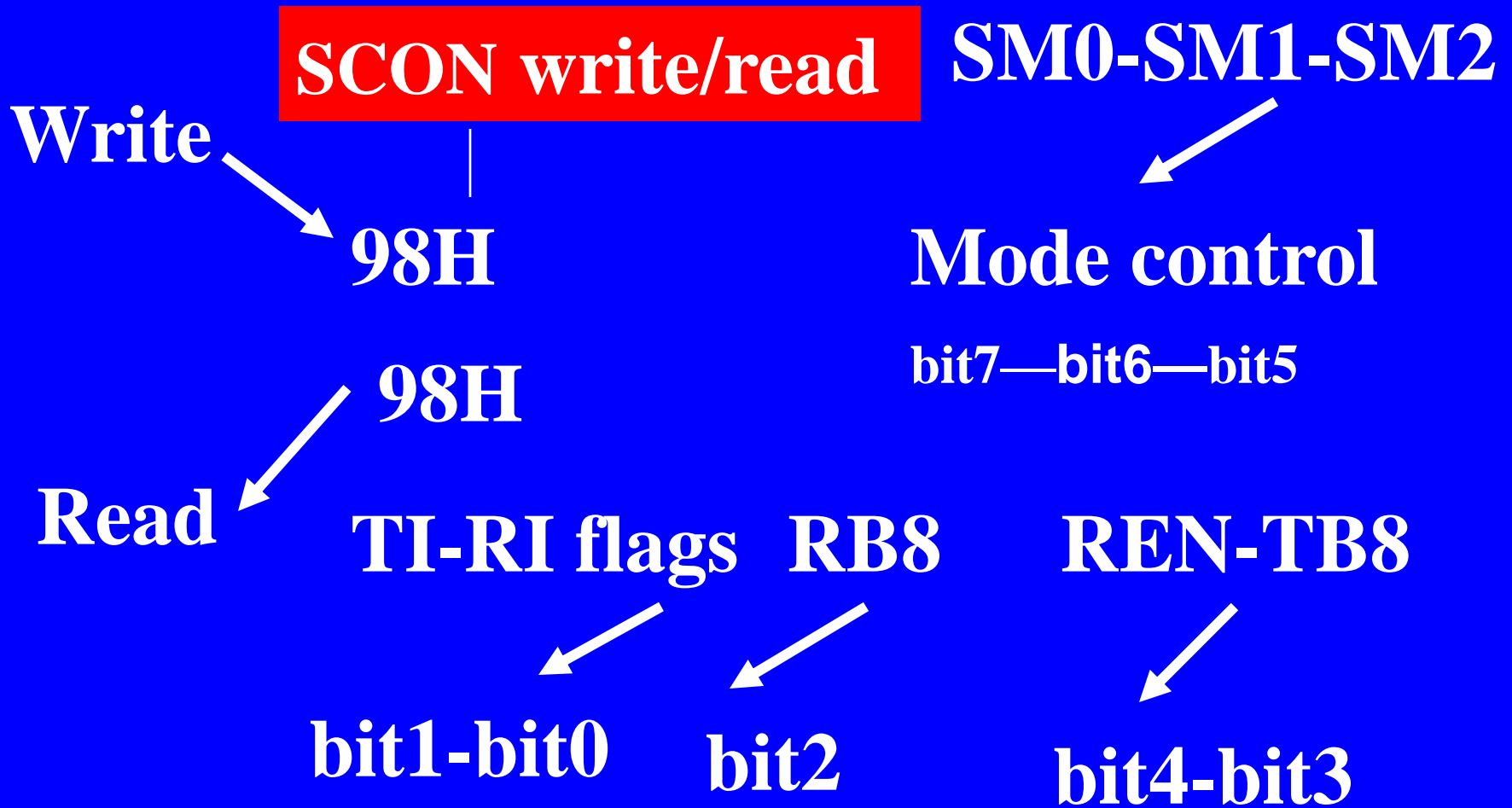
# SFR SBUF Two Windows SBUF - Read and SBUF-Write in

# SI Serial Interface SBUF SFR and Address



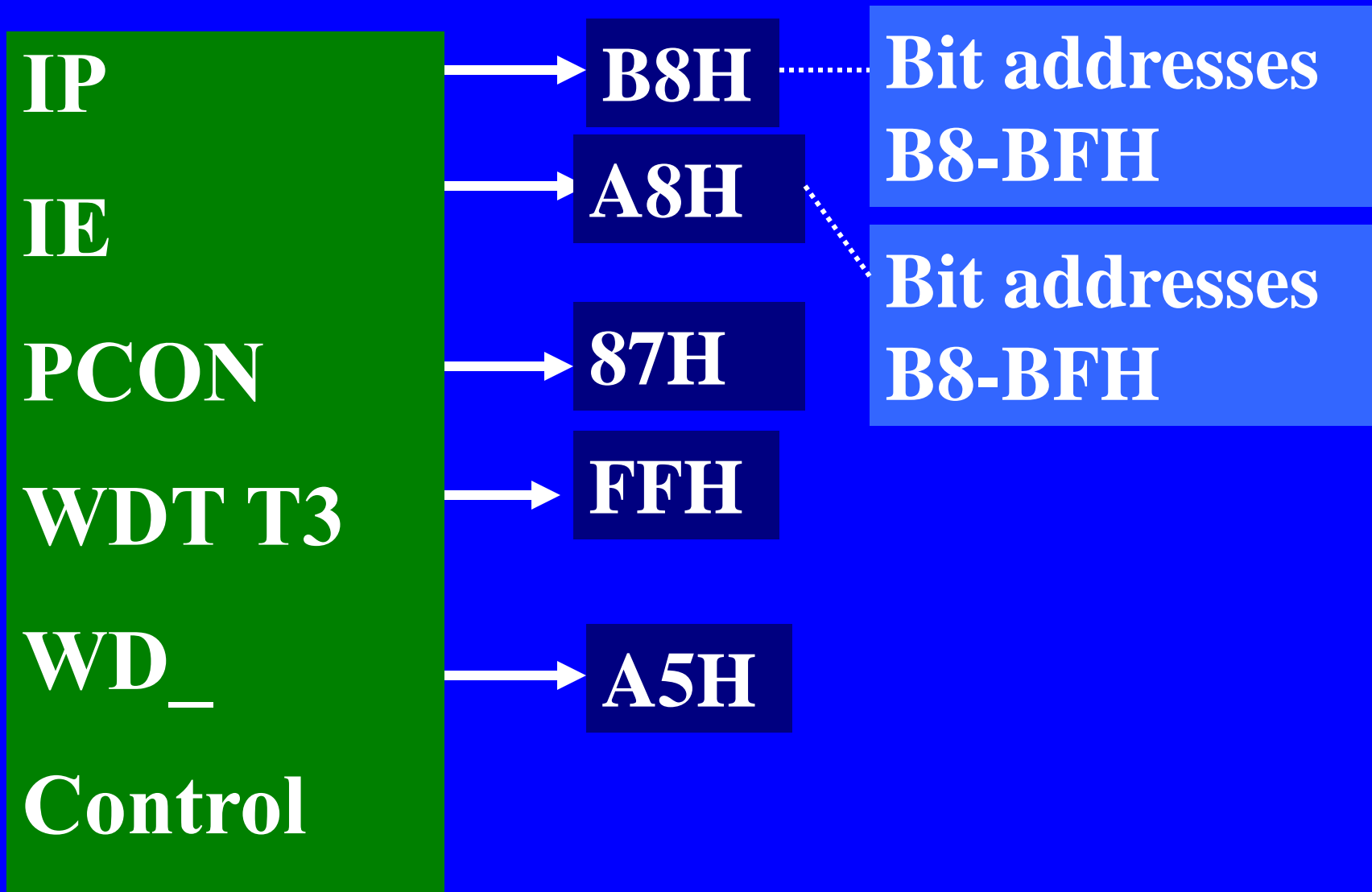
# SI Serial Interface control/status

## SCON SFR and Addresses



# System Function Control SFRs

# System Function Control SFRs



# PCON Power Control SFR Address



PCON (HCMOS)	0XXXXXXXX
PCON (CHMOS)	0XXX0000

# WDT T3 Timer Addresses

Write

WDT T3

FFH

# SFR WDT control Register

**WD\_Control**

**Write**

**A5H**



**No read at A5H**



# Interrupt Control SFRS

- Masks Primary and Secondary IE register
- Interrupt Priority IP register

**IE** Interrupt mask

Primary mask bit  
Enable all

IE.7 IE.6 IE.5 IE.4 IE.3 IE.2 IE.1 IE.0

EA - ET2 ES ET1 EX1 ET0 EX0

**IP** interrupt Priority

IP.7 IP.6 IP.7 IP.6 IP.7 IP.6 IP.7 IP.6

- - PT2 PS PT1 PX1 PT0 PX0

# Summary

# We learnt

## IO Ports

- Port P0, AD0-AD7 option
- Port P2, A8-A15 option
- Port P1, I2C signals and Timer 2 signals options
- Port P3, RxD, TxD, Data, Clock, INT0, INT1, GT0, GT1, T0, T1, Rd, WR signals options

# We learnt

Timer and Serial Device SFRs and their addresses

- TH1-TL0 and TH0-TL0, T2 in 8052
- TMOD
- SBUF
- SCON

# We learnt

## System Control SFRs

- PCON
- WDT T3, WD\_Control
- IE and IP