Chapter 3

8051/8031 Family Architecture

Lesson 2

8051 Family MCUs Memory

Internal and External Memory

Internal memory

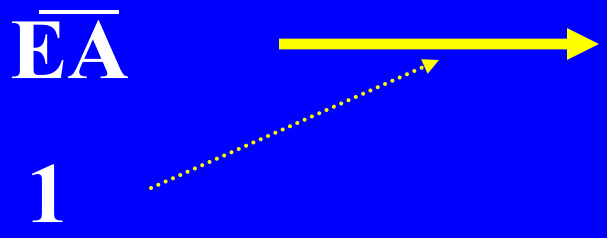
- 8-bit address Internal RAM Memory
- 16-bit address Internal ROM Program memory

- SFRs are separate and have 8-bit address each in separate space from internal RAM

External memory

- 16-bit address Data Memory
- 16-bit address Program memory

Internal Memory Harvard Architecture

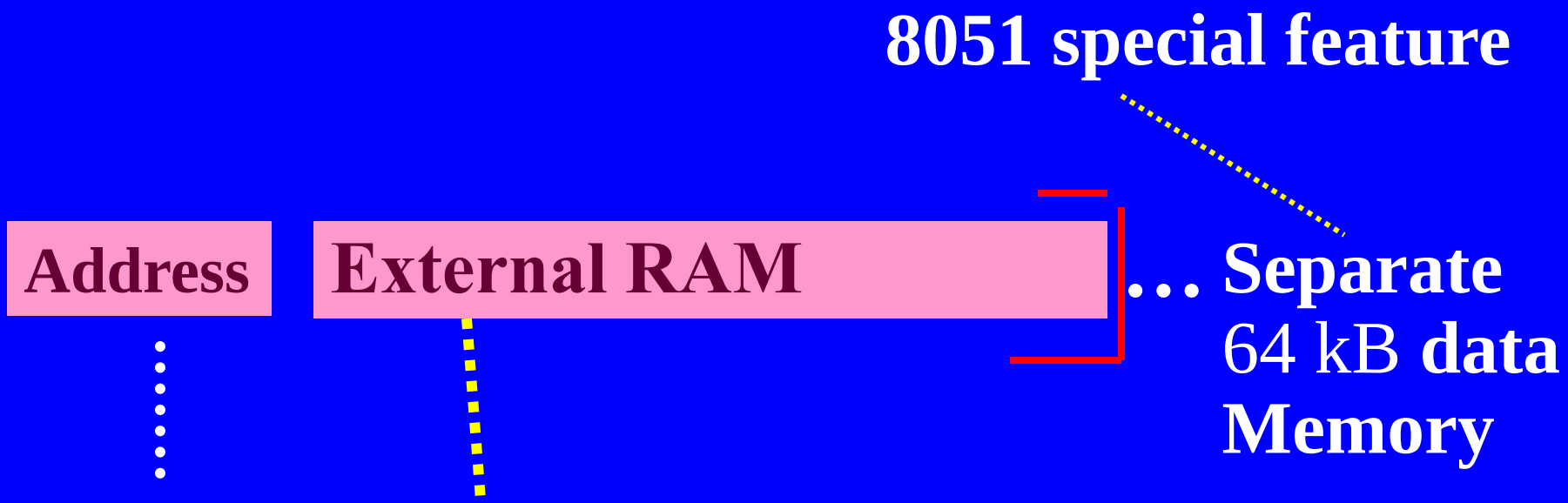


Internal Program Memory (4kB) addresses used when $\overline{EA} = 1$

Internal Data Memory

- 128 B 8051
- 256 B 8052

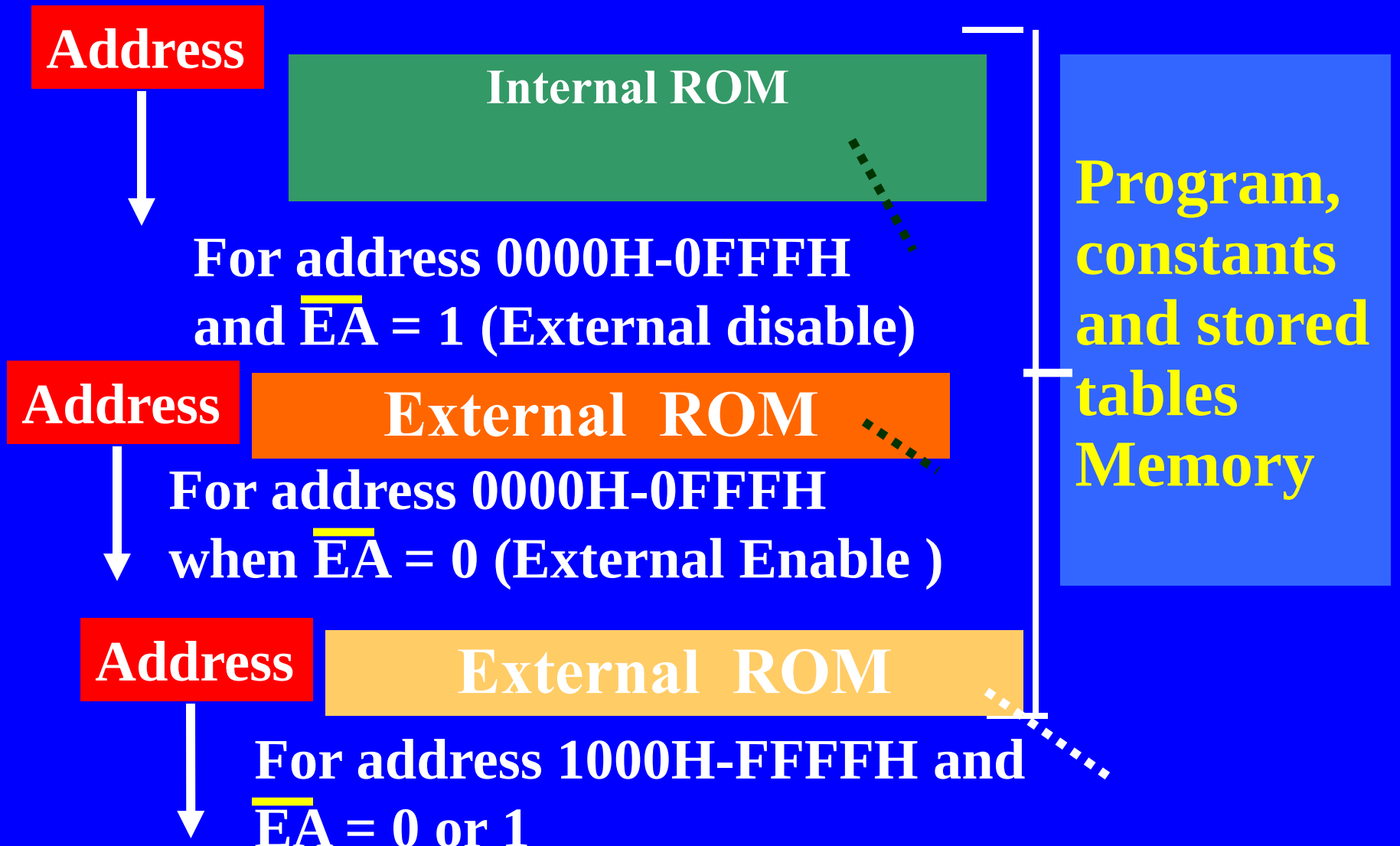
External Data Memory Architecture



64 kB separate address spaces for data memory

Internal/External Program Memory Architecture

Program Memory Architecture

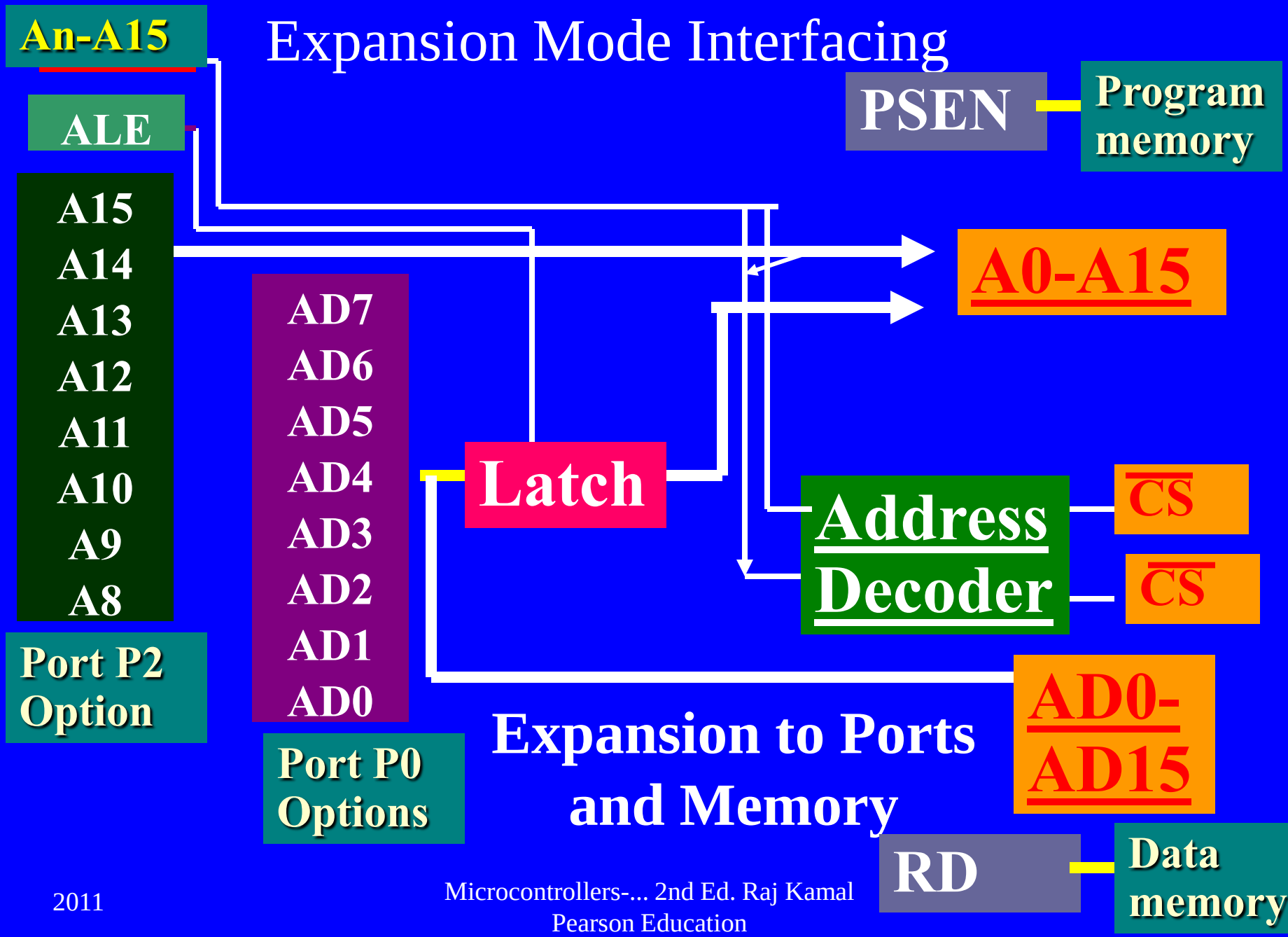


Expansion to external memory and ports

Expanded Mode used for interfacing

- External Data Memory and Ports and
- External Program memory

Expansion Mode Interfacing



On-Chip/Off-Chip Memory Addresses

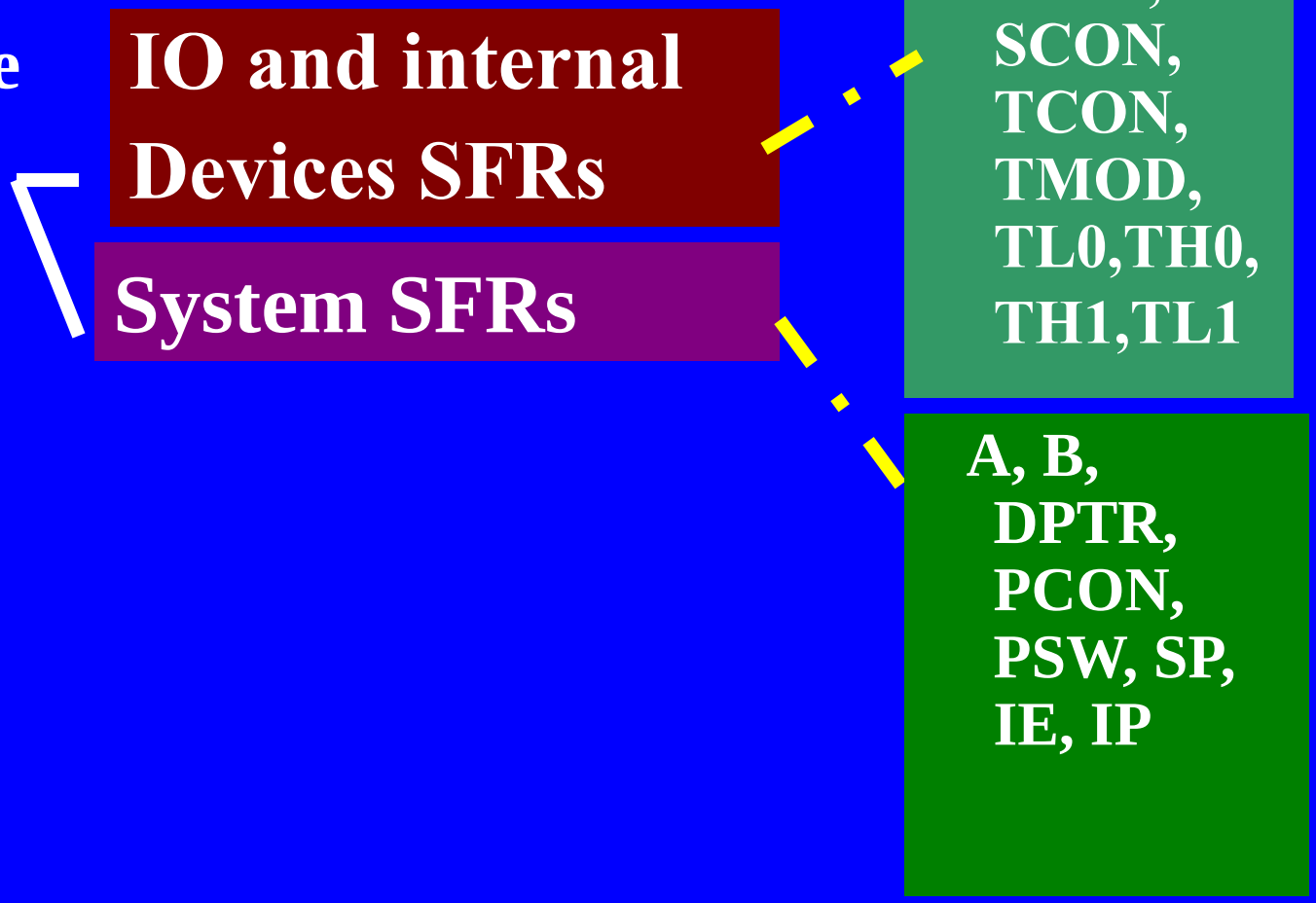
SFRs 80H-FFH

- Used for IO and internal devices Control and Status
- CPU Registers
- Not the part of Internal RAM

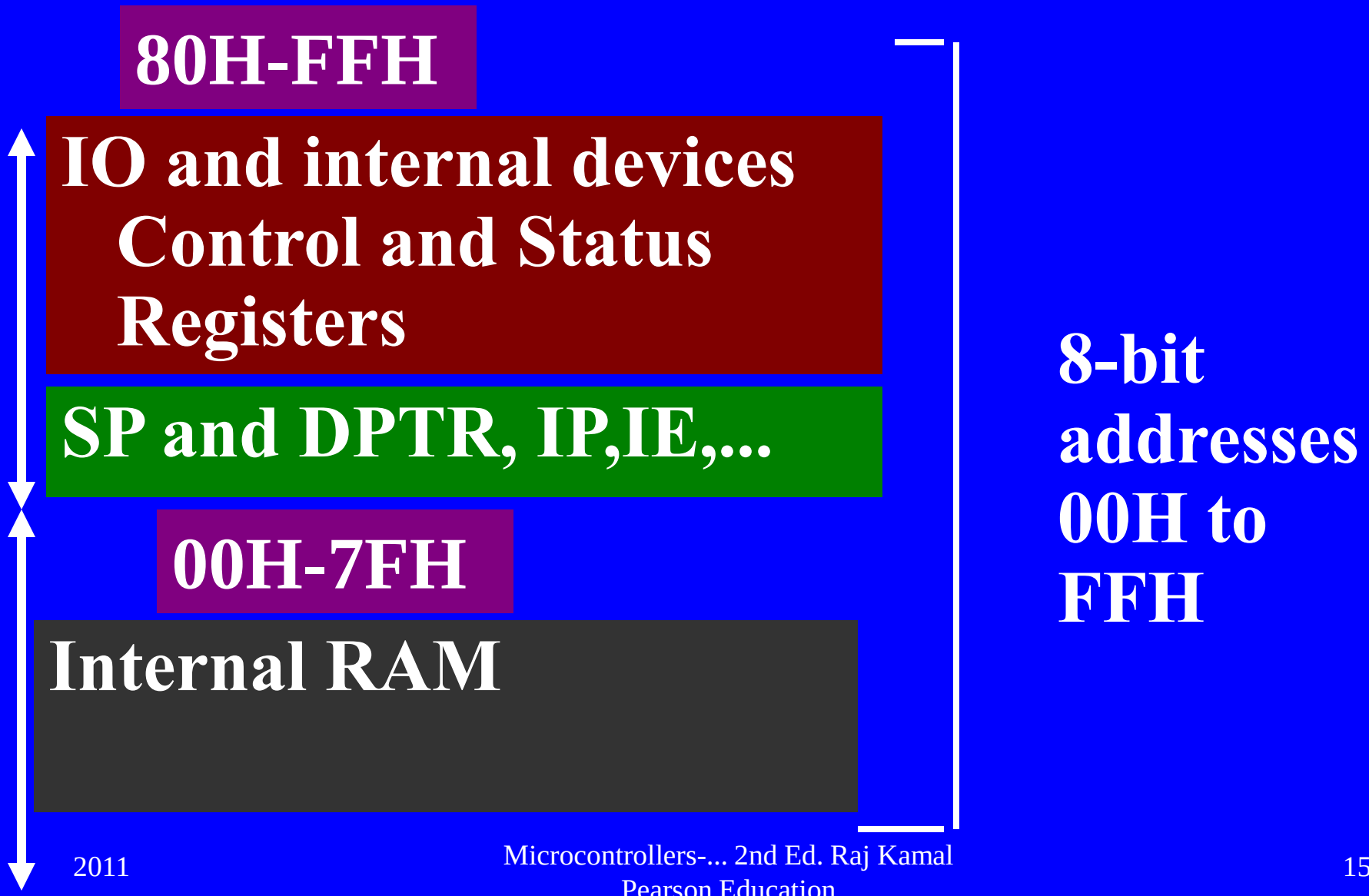
On-Chip SFR and Memory Addresses 8051/52

Address Space

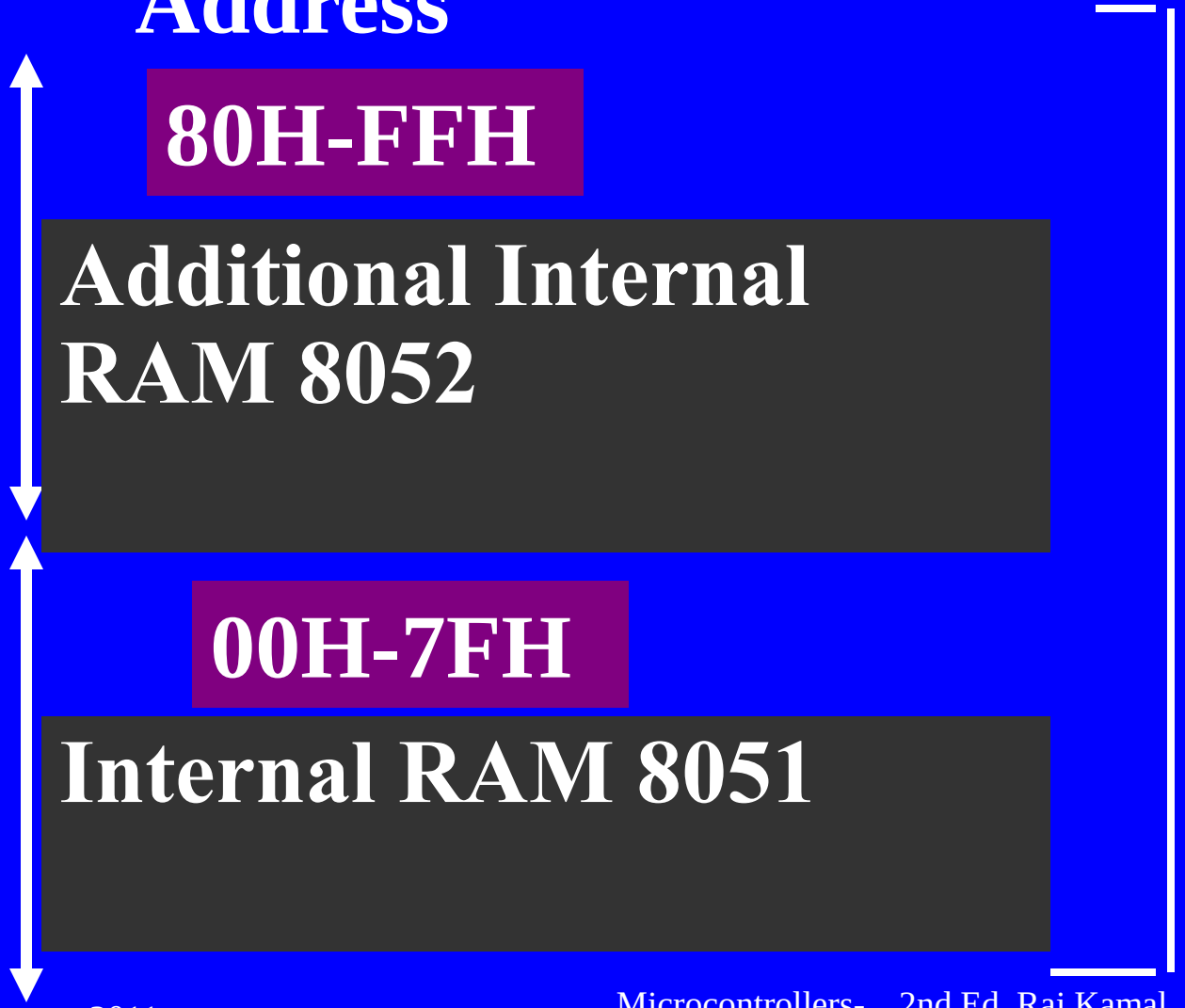
80H-FFH



Memory Access by Direct Address

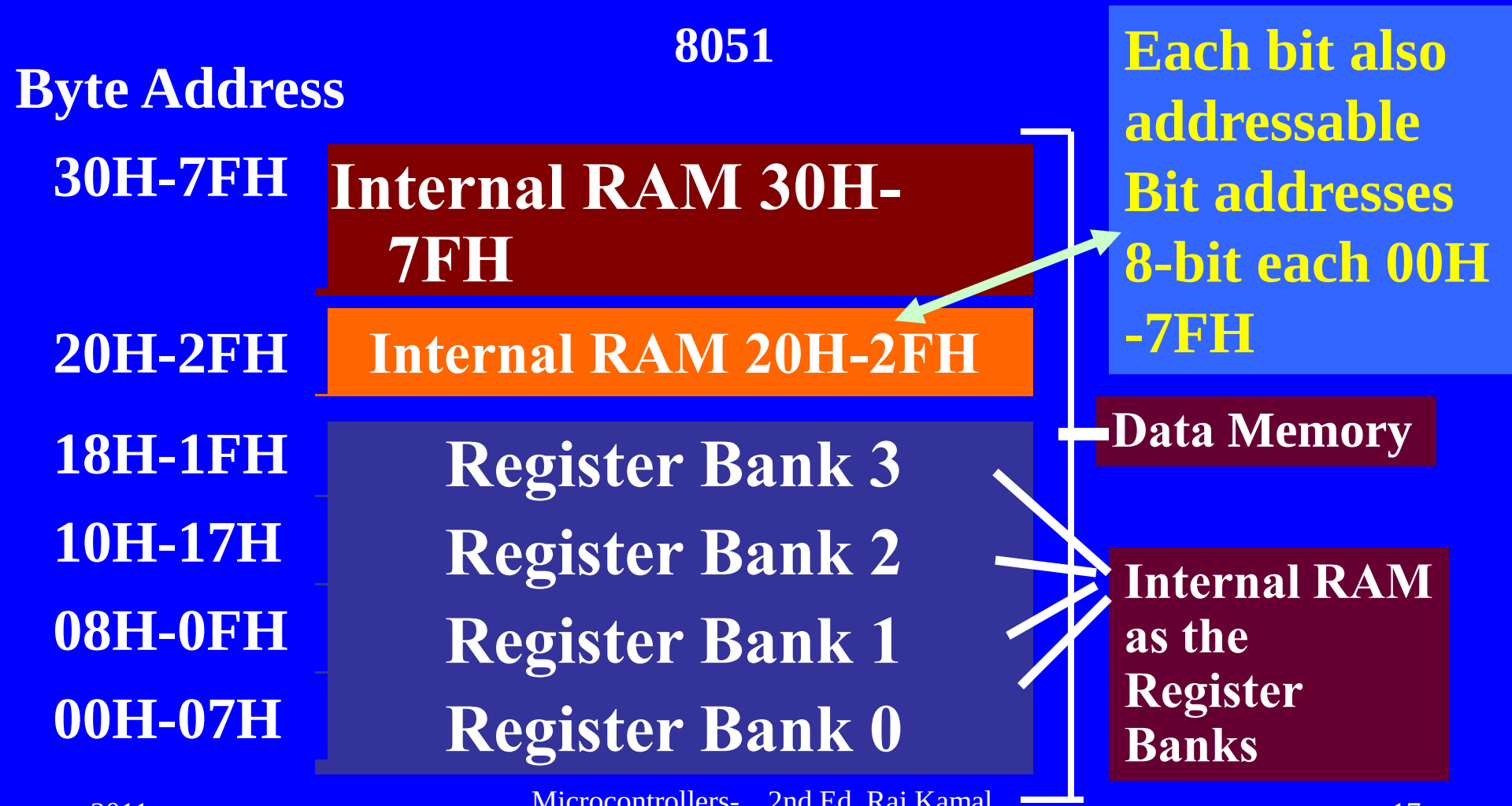


Memory Access by Indirect Address



8-bit addresses 00H to FFH

On-Chip Memory Architecture
Internal Data Memory RAM



Register Banks of 8 registers each

- **Each Byte at the register Ri (R0 orR1) in a register-bank can be used as pointer to an 8-bit indirect addressing**
- **Each Byte at the register R0, .., R7 (R*n*) can be used for a variable with 3 bits in instruction defining *n*** and RS0 and RS1 at PSW defining the bank 0, 1, 2, or 3.

Off-Chip Memory Addresses

8051

0000H-FFFFH External RAM Data Memory

0000H-FFFFH External ROM Program Memory when $\overline{EA} = 0$

1000H-FFFFH External ROM Program Memory when EA = 0 or 1

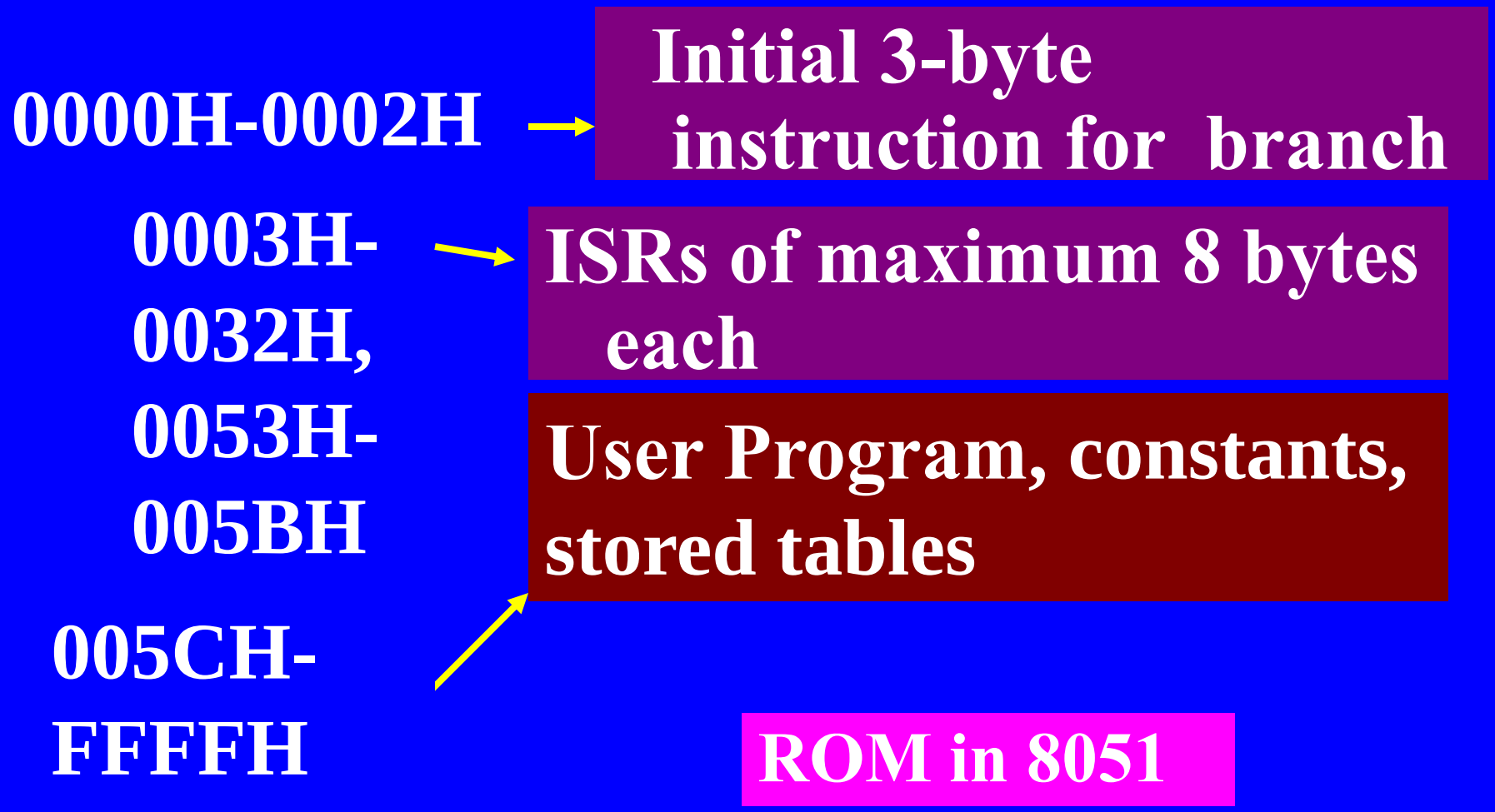
External RAM in 8051

0000H-00FFH → **page0 external RAM, indirect addressable by R0 or R1 or by indirect 16-bit address**

01FFH-FFFFH → **Indirect 16-bit address**

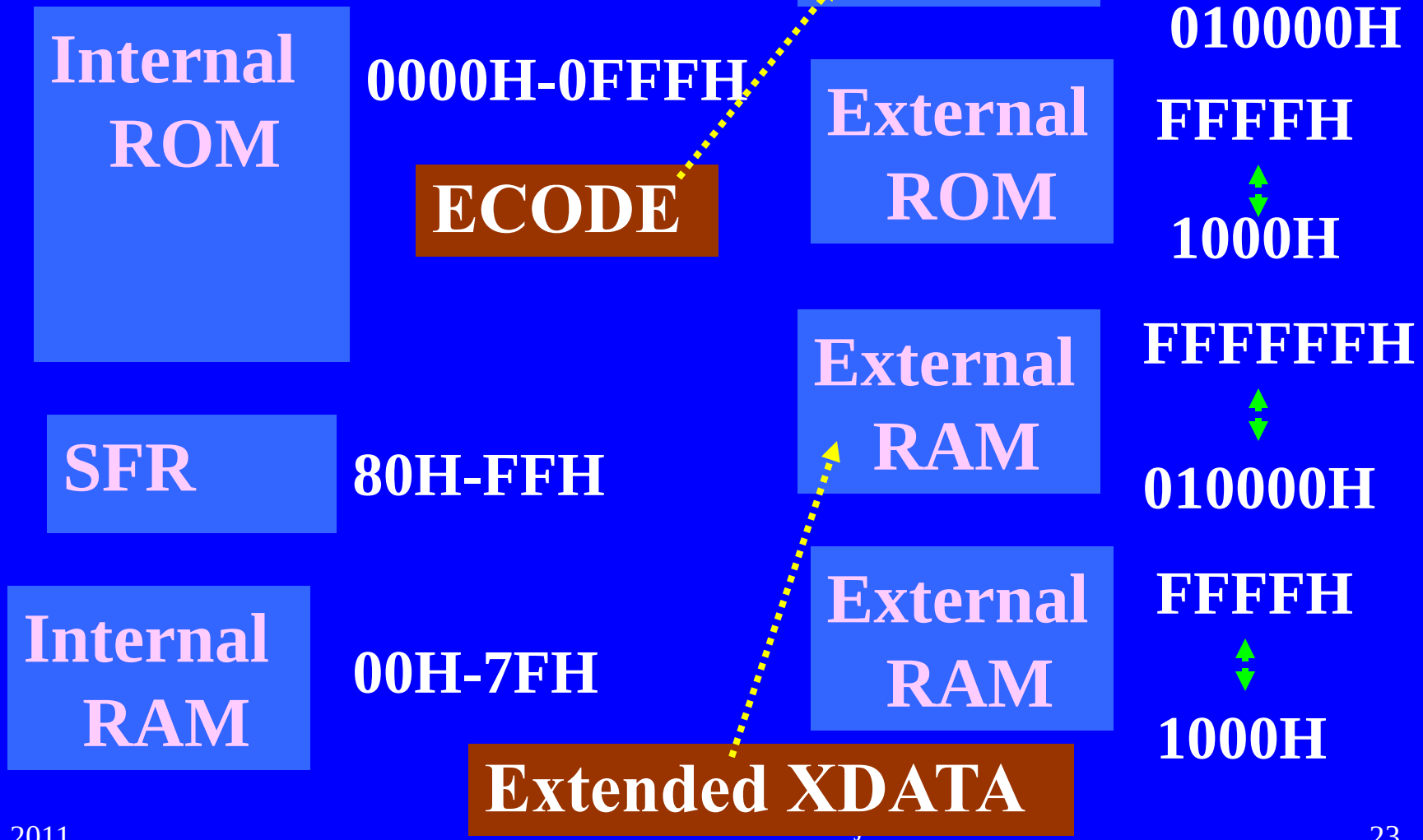
Off-Chip Data Memory Architecture

Program Memory Architecture



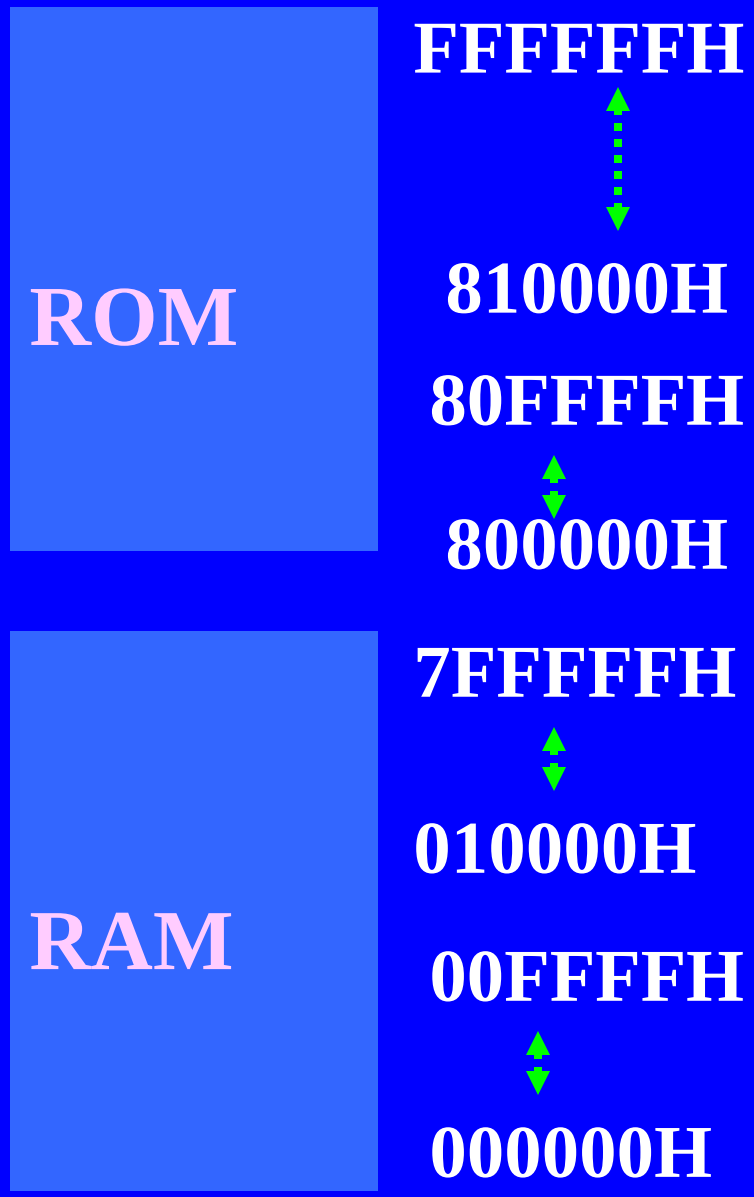
On-Chip/Off-Chip Memory Addresses in extended 8051

Extended 8051

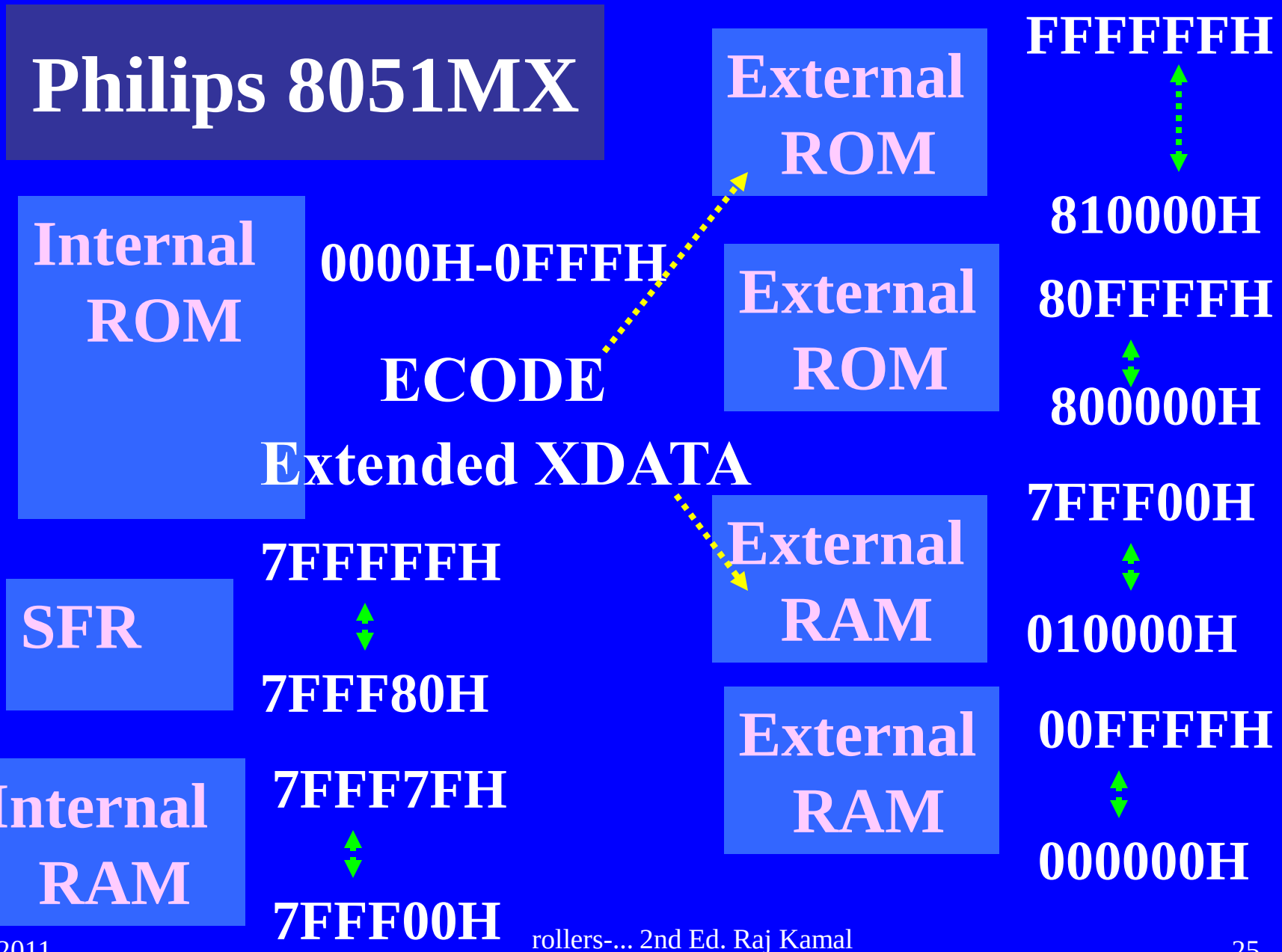


Philips 8051MX

Unified Internal and External Addresses Princeton Architecture



Philips 8051MX



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Summary

We learnt

SFRs and memory

- SFRs
- Internal RAM with bit addressable RAM and four register banks
- External RAM - Harvard Architecture
- Internal Program Memory - Harvard Architecture
- External Program Memory - Harvard Architecture

We learnt

memory

- Extended Memory in Extended 8051 version
- Unified Memory space in 8051MX