Chapter 3

8051/8031 Family Architecture

Lesson 1

8051/8031Architecture overview

CPU Feature and Special Function Registers

8051 **Special Function Registers**

- CPU (A, B, SP, PSW, DPL, DPH)
- Registers associated with the, Internal-devices, Ports

CPU Registers

- 8- bit A (Accumulator) Register
- 8-bit B Register
- 8- bit PSW (Processor Status Word)
- 8-bit Stack Pointer SP

CPU Registers Common Uses

A as Accumulator in instructions

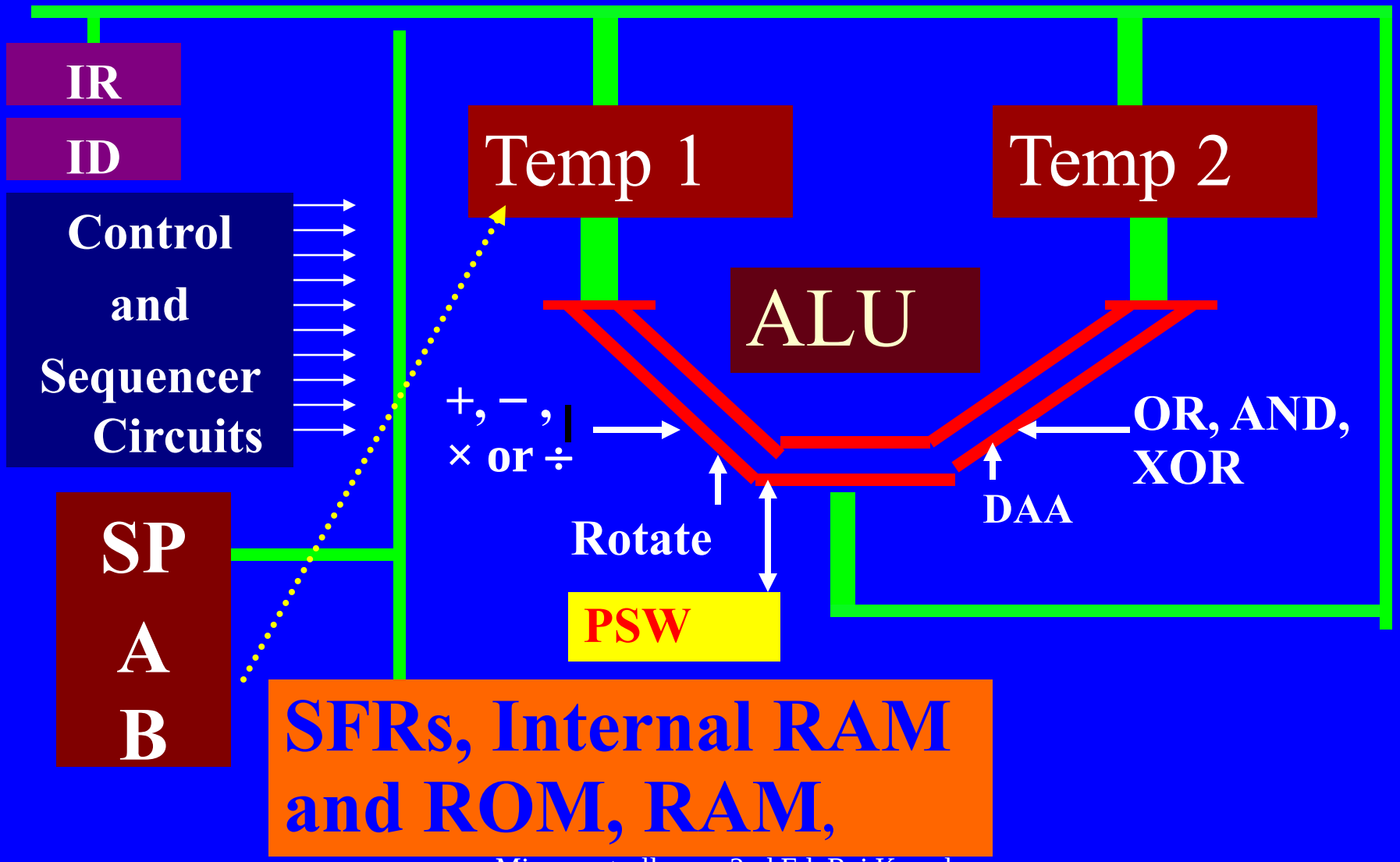
- B for MUL and DIV
- PSW for Processor Status Word for flag bits and register-bank selection bits
- SP for stack at internal memory

Pointer 16-bit Registers

- 16-bit Program Counter PC to point to instruction byte in program memory
- 16-bit Data Pointer DPTR points a byte in external data memory
- DPTR two bytes in DPH and DPL SFRs

Execution Unit- ALU

Execution Unit



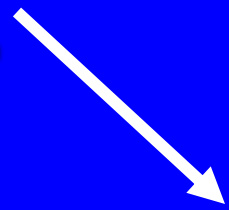
- Instructions have **8 -bit** data types

PSW

PSW.0	P	Zero flag
PSW.1	F1	User Flag1
PSW.2	OV	Overflow flag
PSW.3	RS0	Register bank select bit0
PSW.4	RS1	Register bank select bit1
PSW.5	F0	Flag 0 of user
PSW.6	AC	Auxiliary Carry
PSW.7	C	Carry flag

Default value
= All 0s

PC

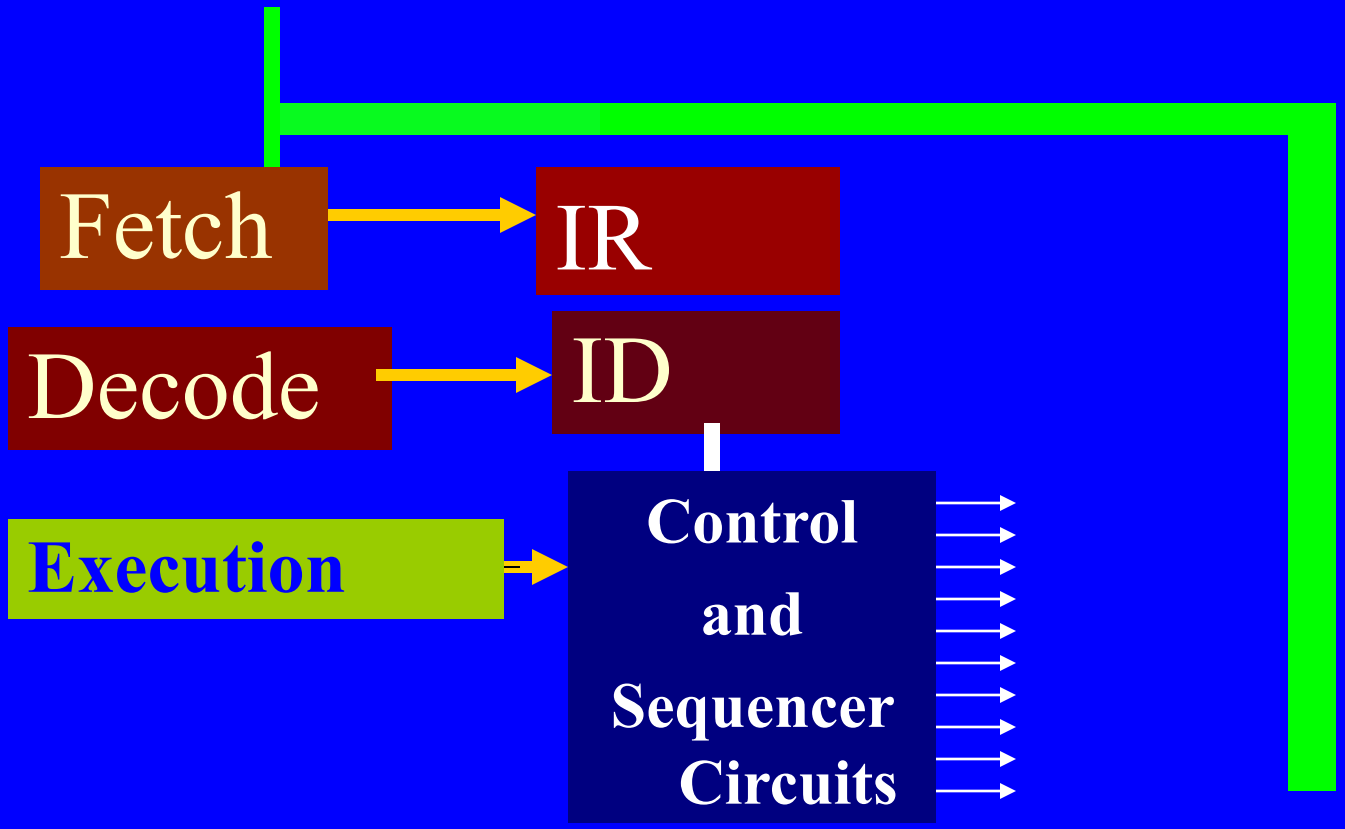


Default value
= 0000H

Not an SFR

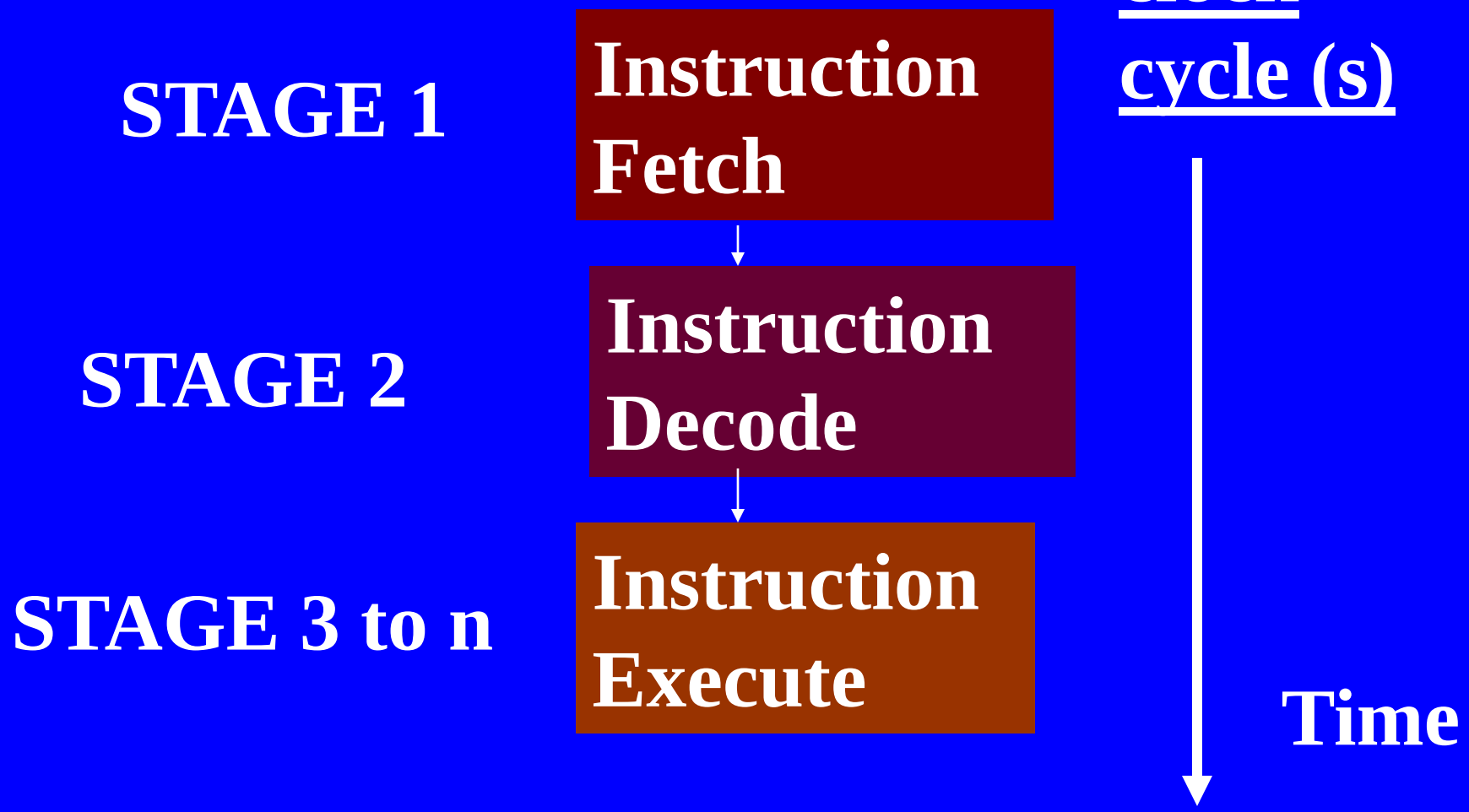
Increases by 01H for next instruction fetch

Internal bus



Control memory micro codes based - Implementation

Instruction Execution

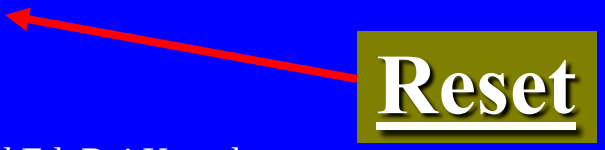


MCU Architecture overview

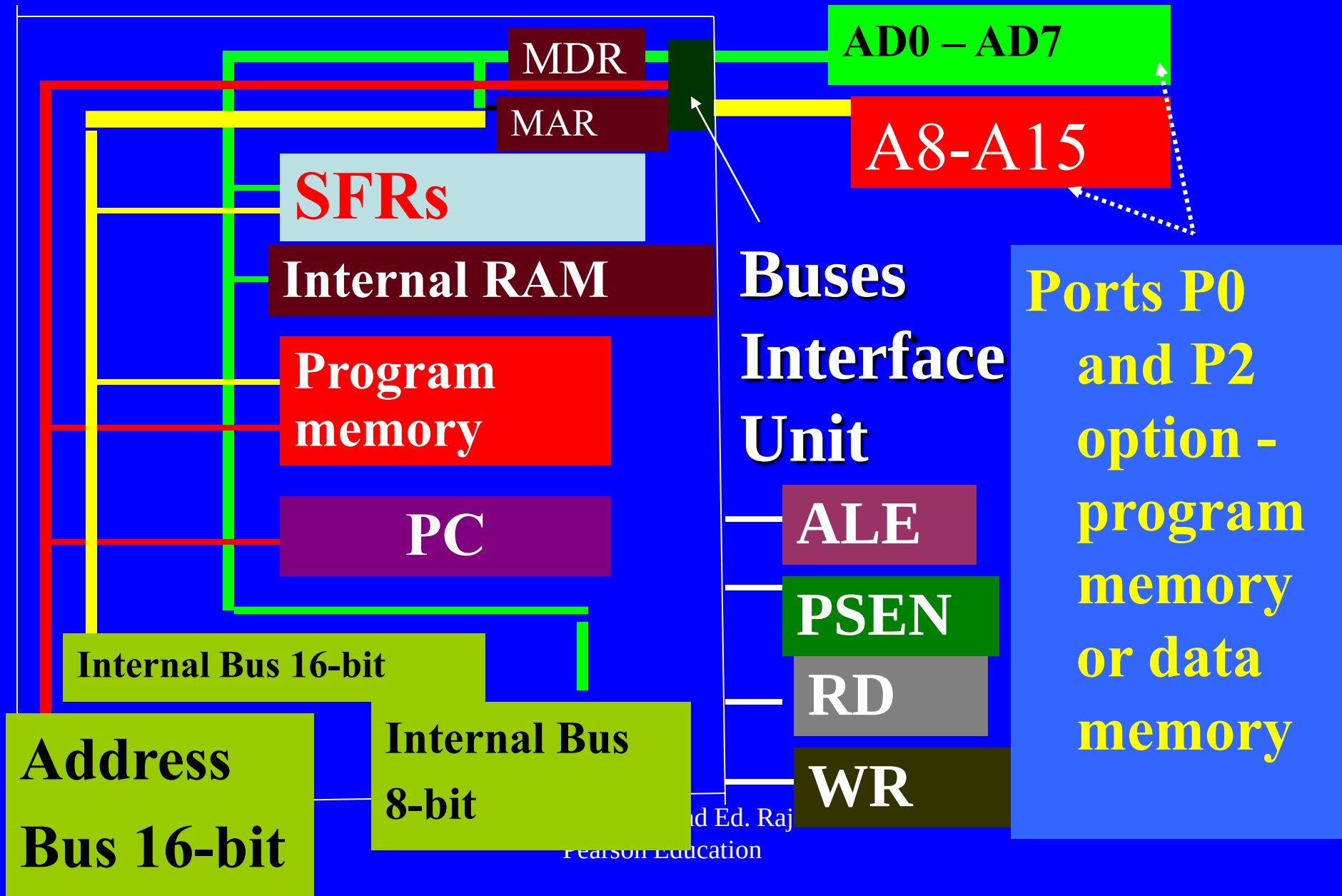
Buses and Cycle Time

- 8-bit and 16-bit internal buses separate for data memory and SFRs, and program memory
- 16 bit address and 8 bits external data buses to program and data memoy
- 12 MHz XTAL- Clock rate 1MHz, 1 μs single instruction cycle time.

- 8051 separate 16-bit internal bus for the 16-bit addressing and separate 8-bit data bus
- Harvard architecture bus
- Bus interface for 16-bit/8-bit address, data and instructions.
- Two Maskable Interrupt requests $\overline{\text{INT1}}$ at P3.3 Interrupt and $\overline{\text{INT0}}$
- PC initialization 0000H



Internal and External Buses



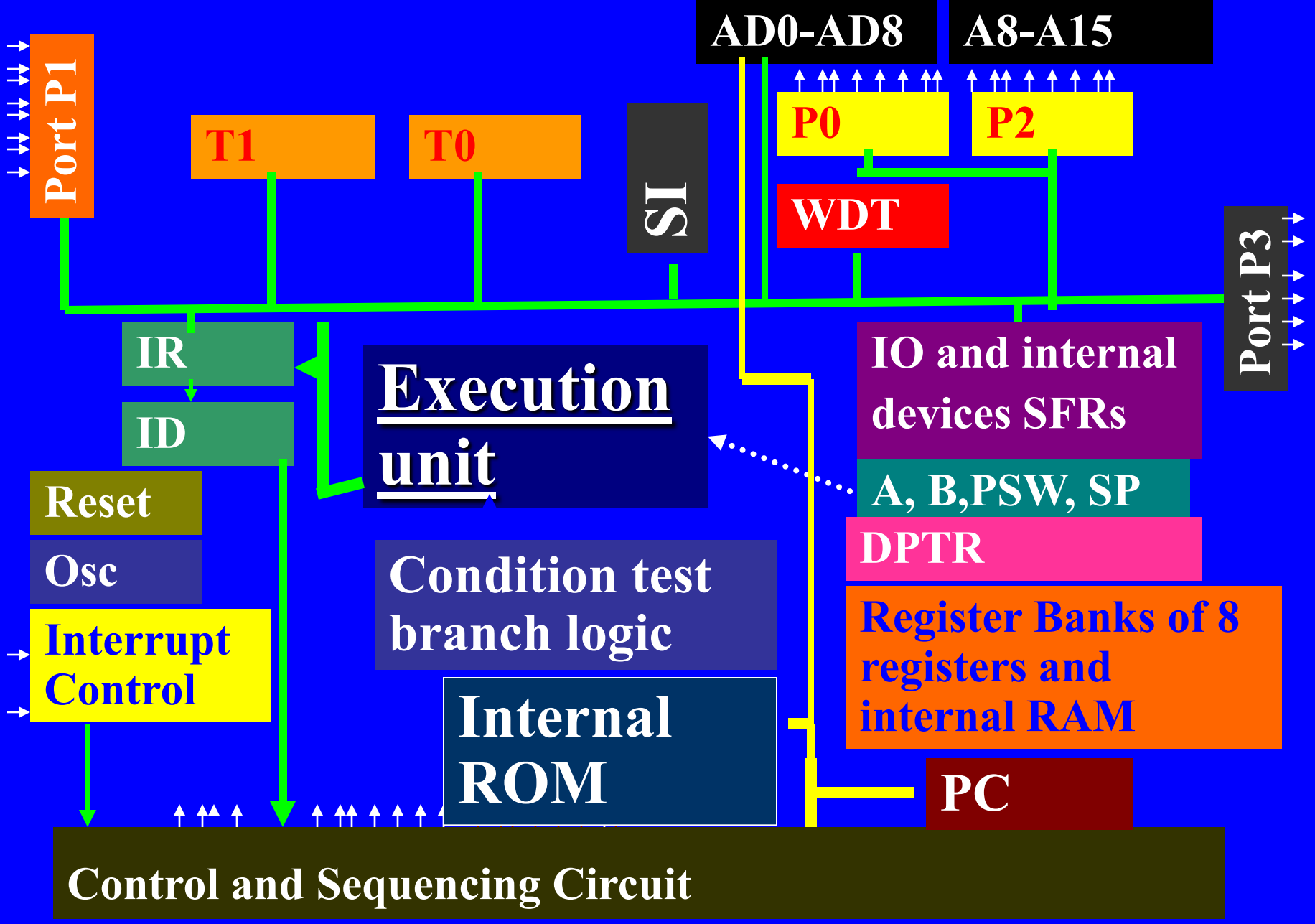
Internal Devices

- Timers T0 andT1 timer with reset, internal/external clocking inputs and load/auto reload
- A watchdog timer

Internal Devices

- Serial Interface SI-option UART full duplex or half duplex serial synchronous bits with separate clock bits

8051 Architecture view


AD0-AD8
A8-A15
Port P1
T1
T0
SI
P0
P2
WDT
Port P3
IR
ID
Execution unit
IO and internal devices SFRs
A, B,PSW, SP
DPTR
Reset
Osc
Interrupt Control
Condition test branch logic
Register Banks of 8 registers and internal RAM
Internal ROM
PC
Control and Sequencing Circuit

Special Function Registers (SFRs) and Internal RAM

- SFR A, B, PSW bytes also have the 8-bit address for each bit like an internal device or port
- An SFR address space is distinct from an Internal RAM address.Byte at SFR has an 8-bit address.
- Select bits at SFR and select bits at internal RAM are individually addressable

PSW

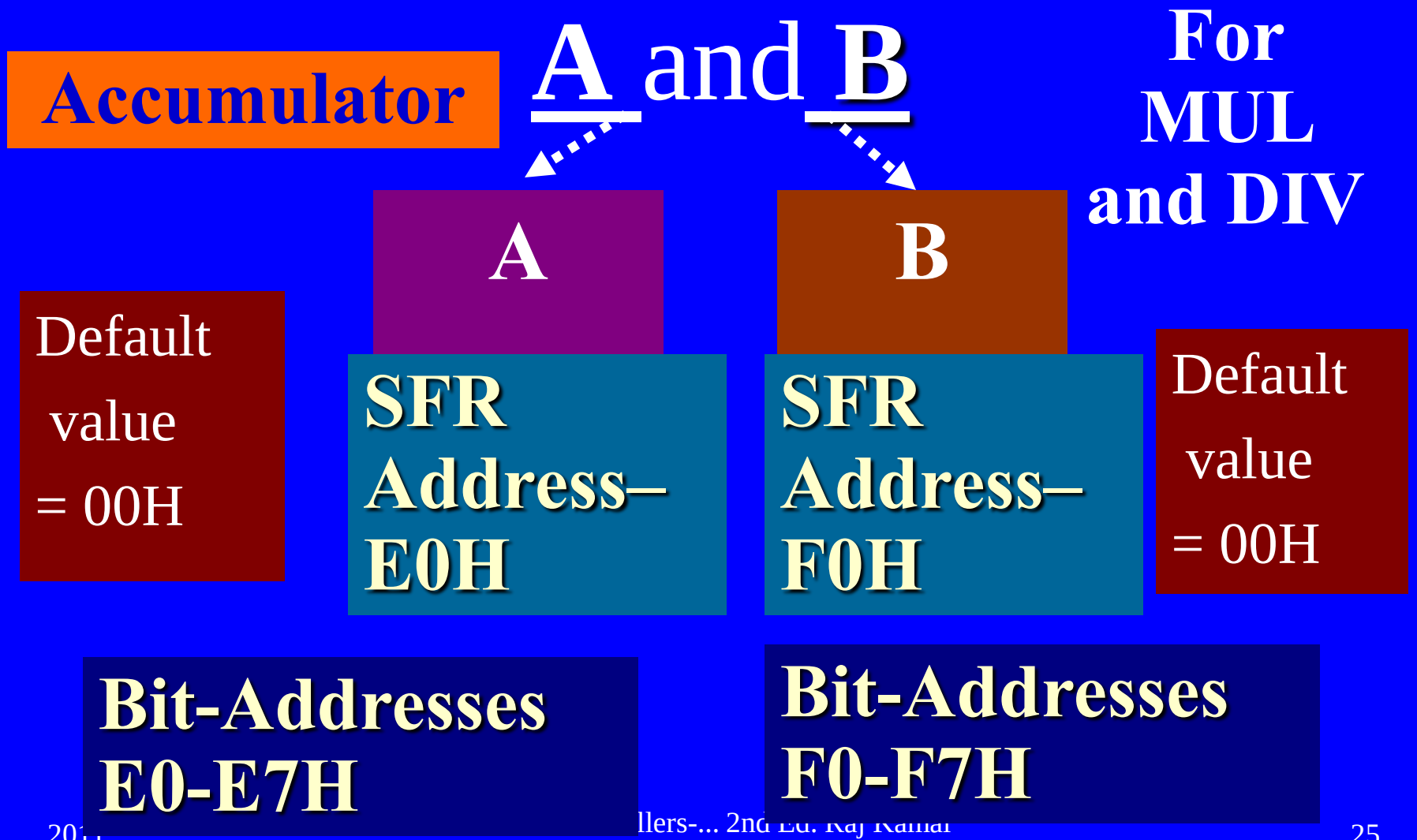
Bit- Addresses	
D7H	PSW.7
D6H	PSW.6
D5H	PSW.5
D4H	PSW.4
D3H	PSW.3
D2H	PSW.2
D1H	PSW.1
D9H	PSW.0

PSW.7 ..... PSW.0

Default value = All 0s

Byte Address = D0H

PSW.7-PSW.0


Accumulator
A and B
For MUL and DIV
A
B
Default value = 00H
SFR Address– E0H
SFR Address– F0H
Default value = 00H
Bit-Addresses E0-E7H
Bit-Addresses F0-F7H

SP

Default value = 07H

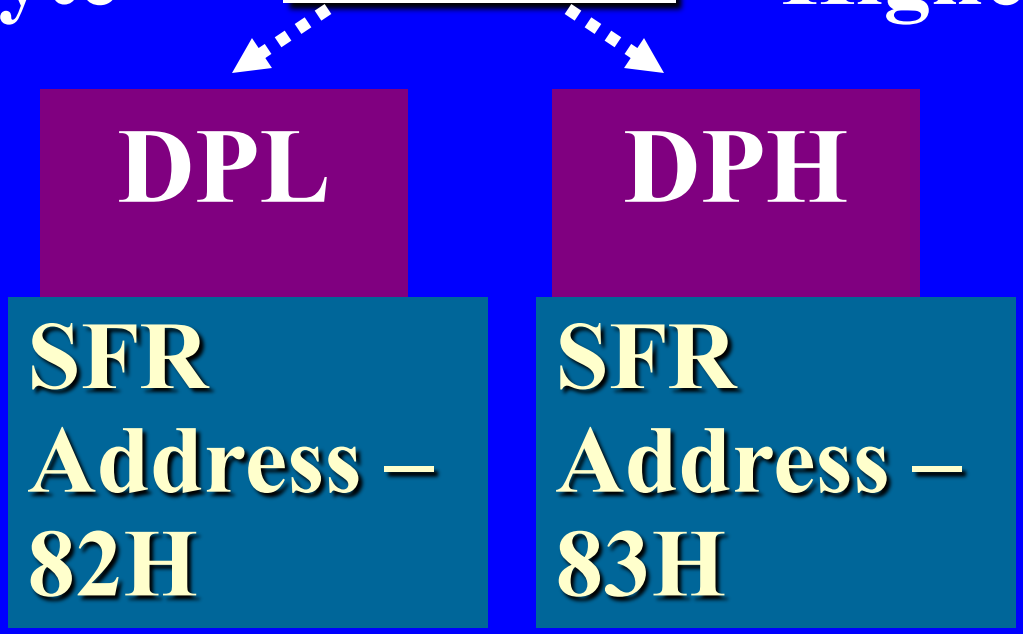
SFR Address – 81H

Increases by 01H before push, decreases after pop by 01H

DPTR

Lower byte

Higher byte

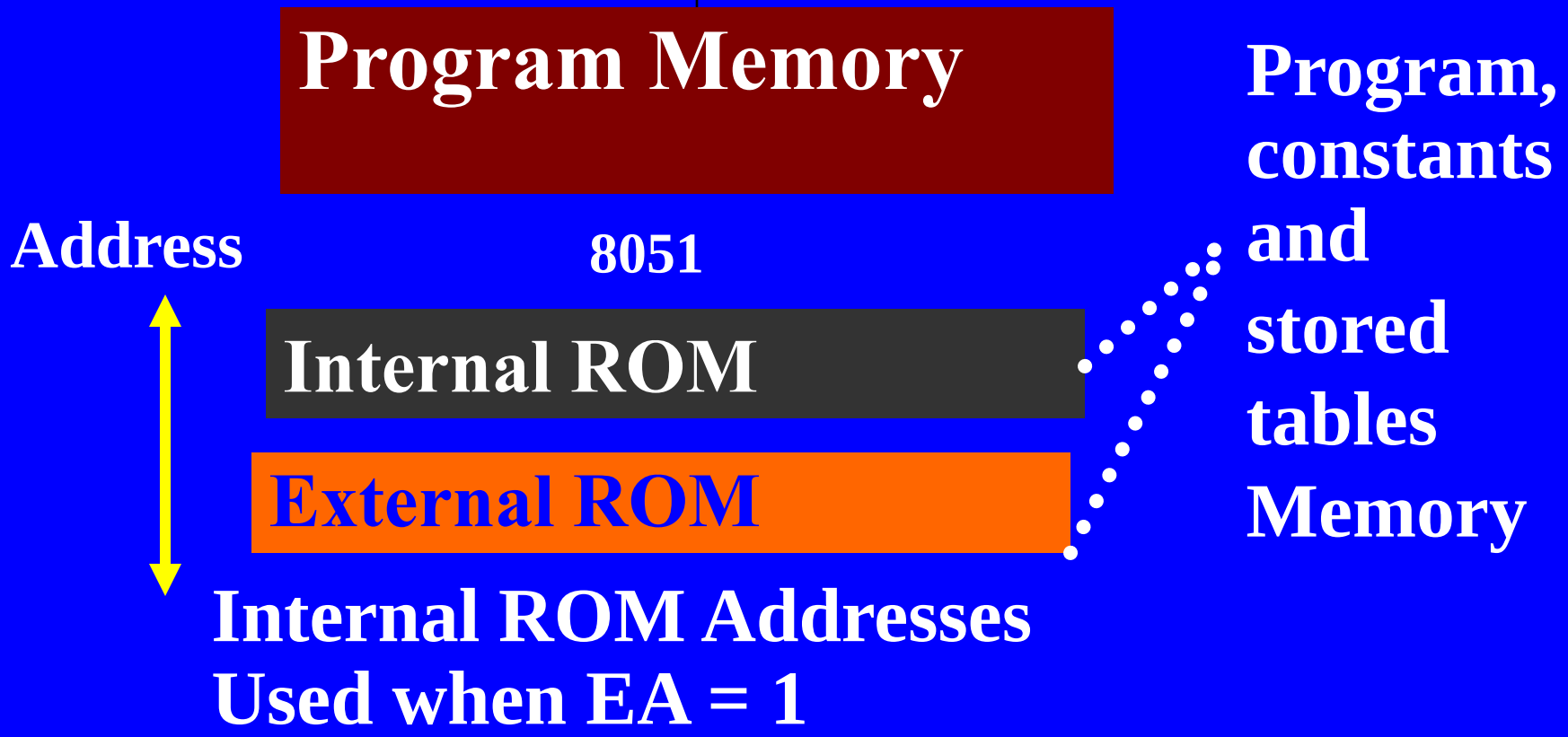


Default value = 0000H

Data Memory address Pointer

Program Memory Architecture

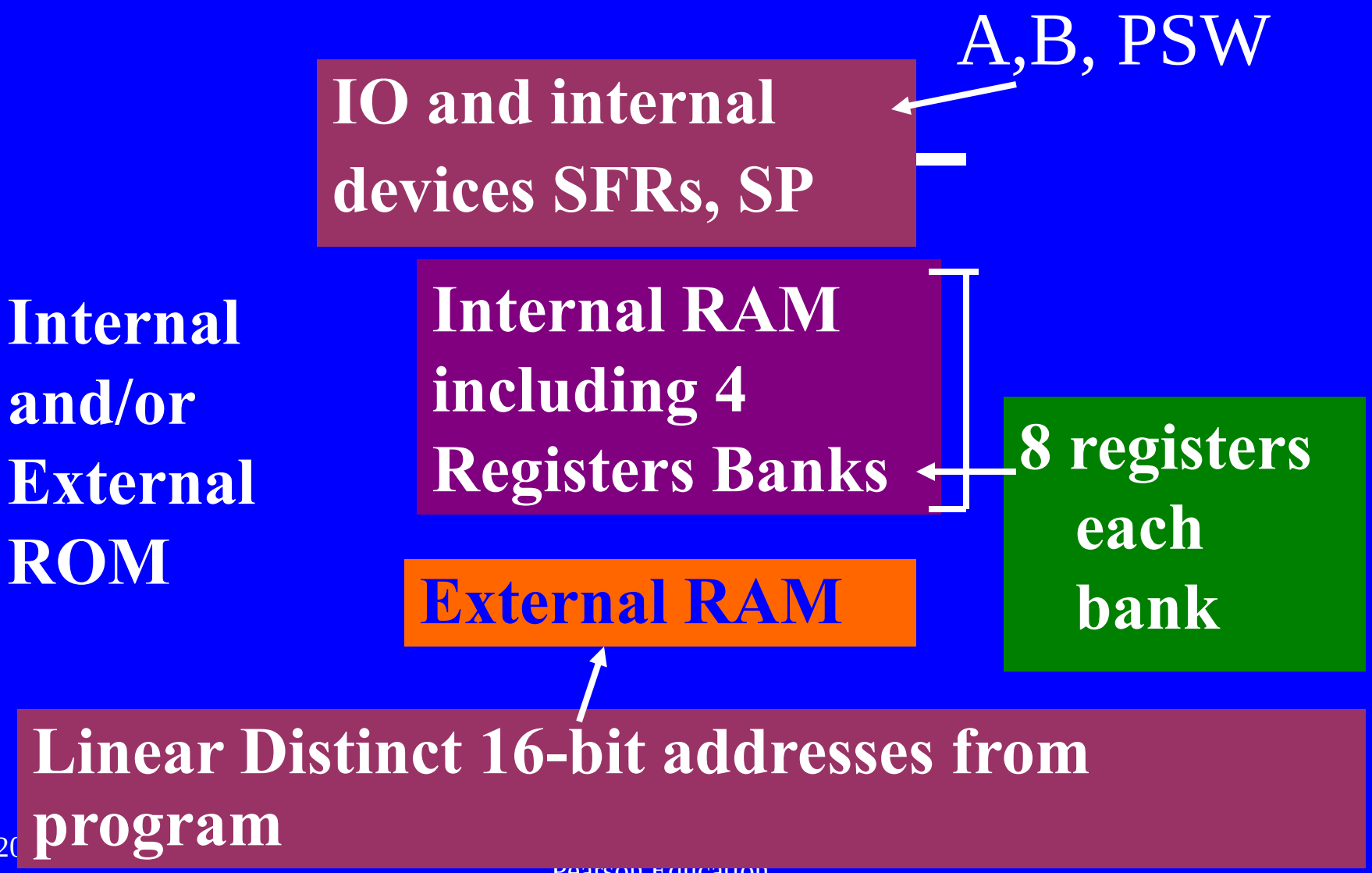
64 kB separate address spaces for program from data memory



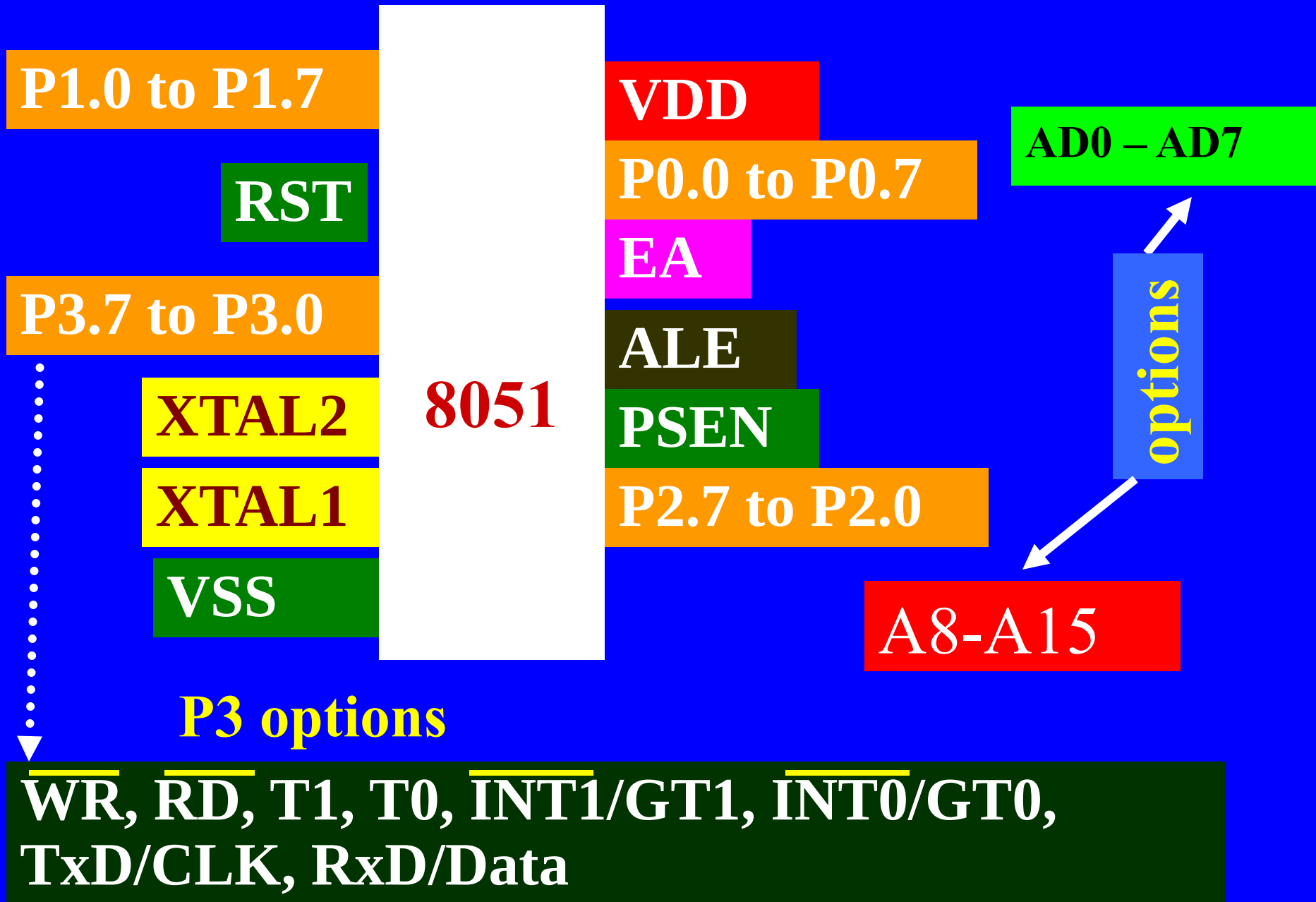
Internal Data and SFRs Architecture

- **Separate** 64 kB **External data Memory**

8051 Family Programming Model



8051 Pins

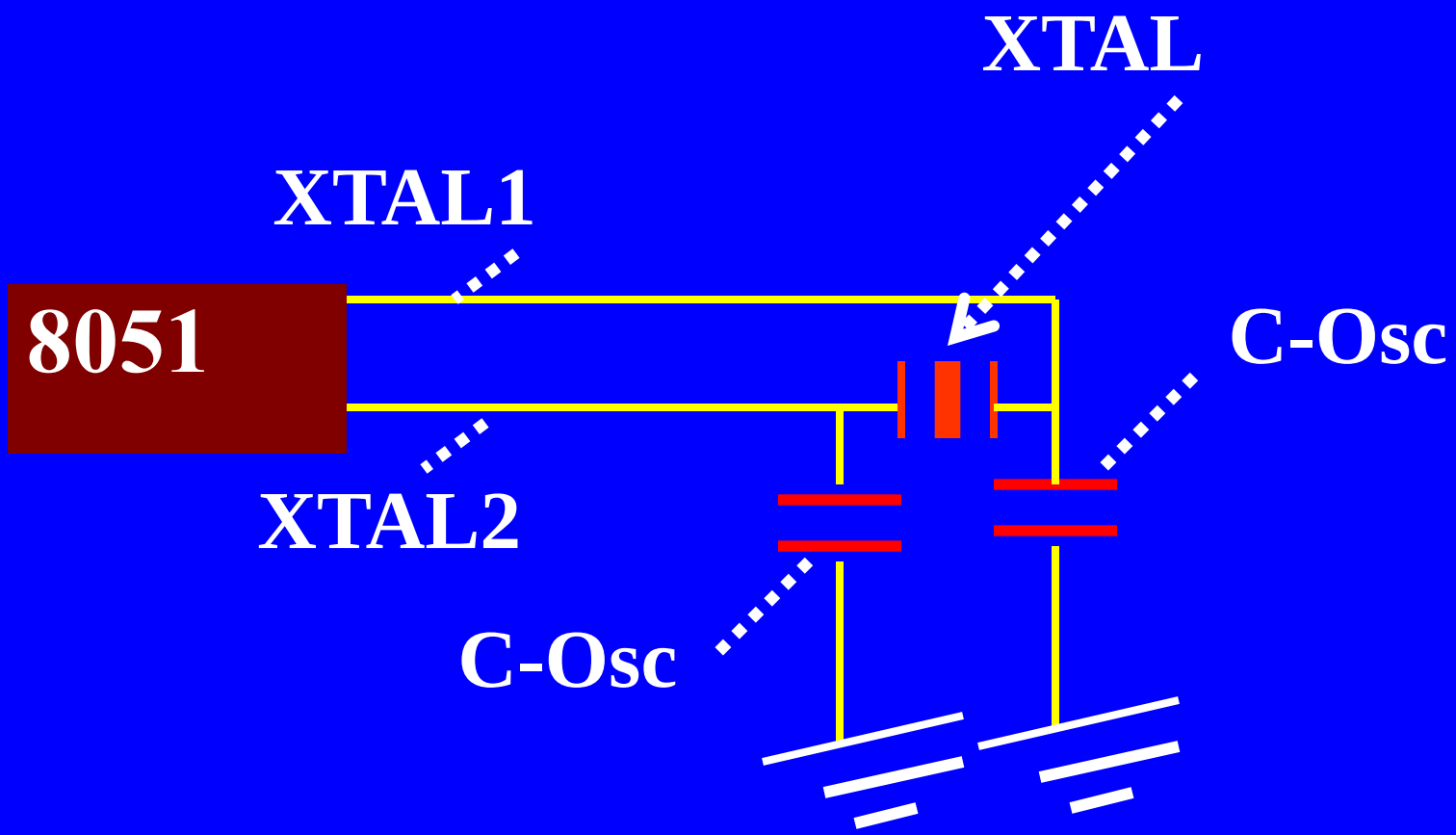

P1.0 to P1.7
RST
P3.7 to P3.0
XTAL2
XTAL1
VSS
8051
VDD
P0.0 to P0.7
EA
ALE
PSEN
P2.7 to P2.0
AD0 – AD7
options
A8-A15
P3 options
WR, RD, T1, T0, INT1/GT1, INT0/GT0,
TxD/CLK, RxD/Data

EA, ALE, PSEN

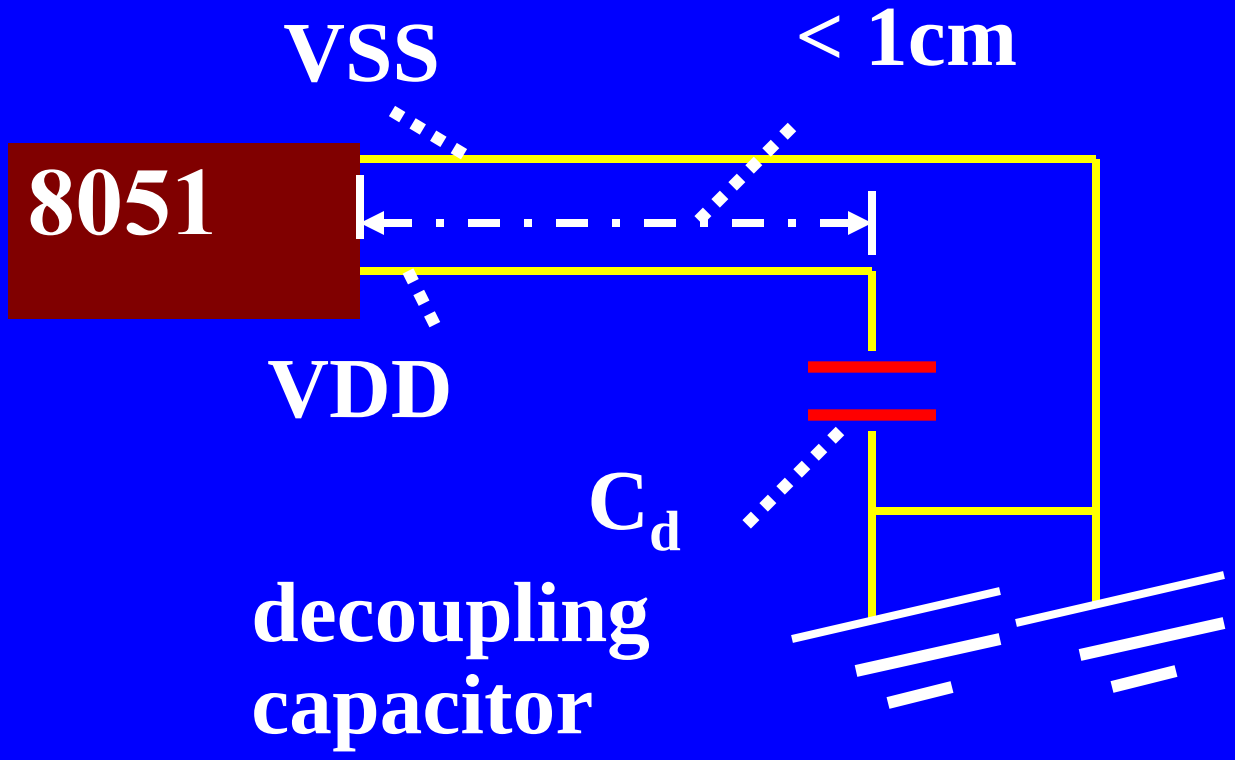
- **$\overline{\text{EA}}$** is made 0 by user to enable use of external program memory space in place of the internal program memory space
- Control signal **ALE** = 1 to enable latching of address A0-A7 bits from AD0-AD7
- Control signal **$\overline{\text{PSEN}}$** = 0 to enable read of program memory bits from external program memory

Oscillator Circuit, Supply circuit

Oscillator Circuit

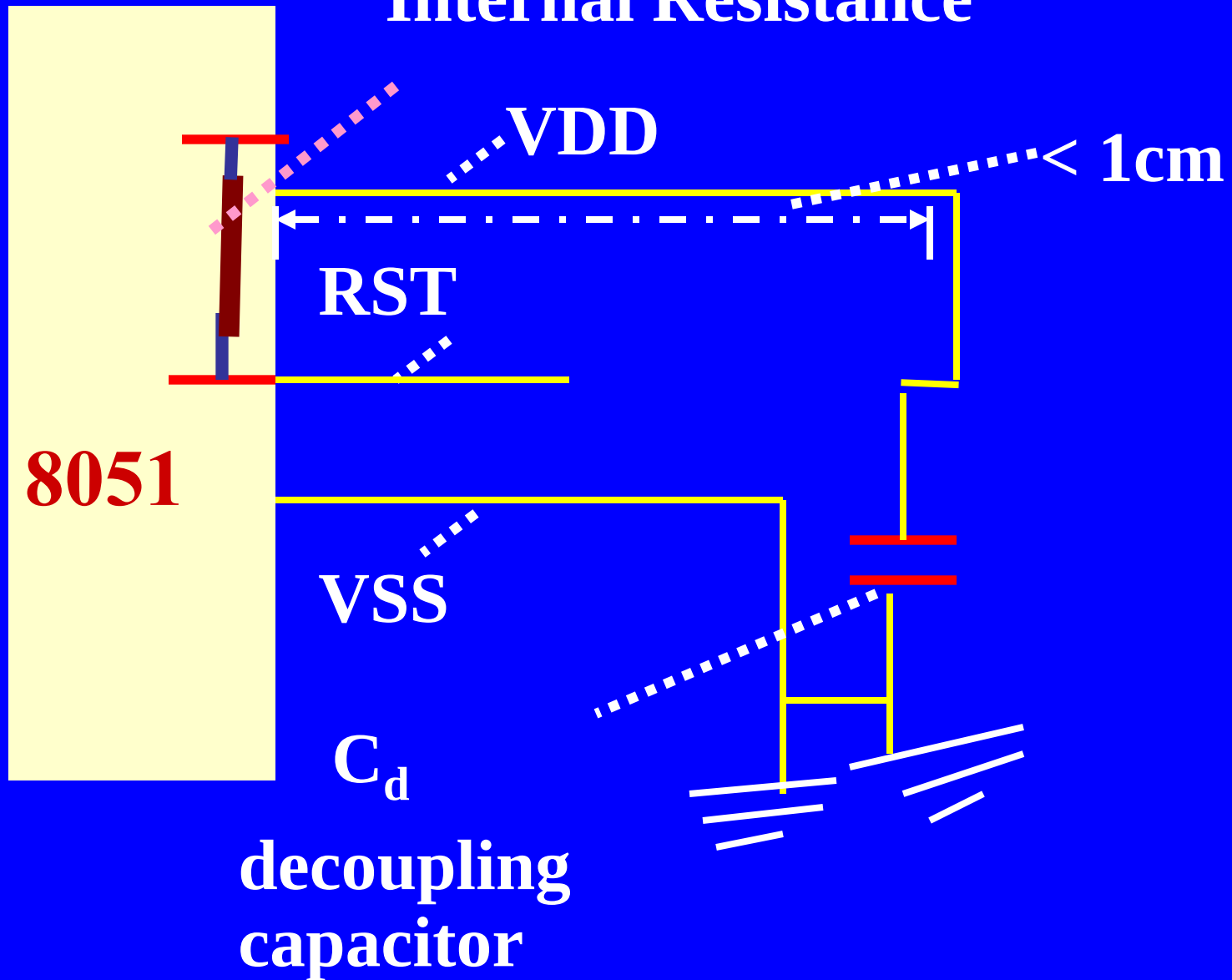


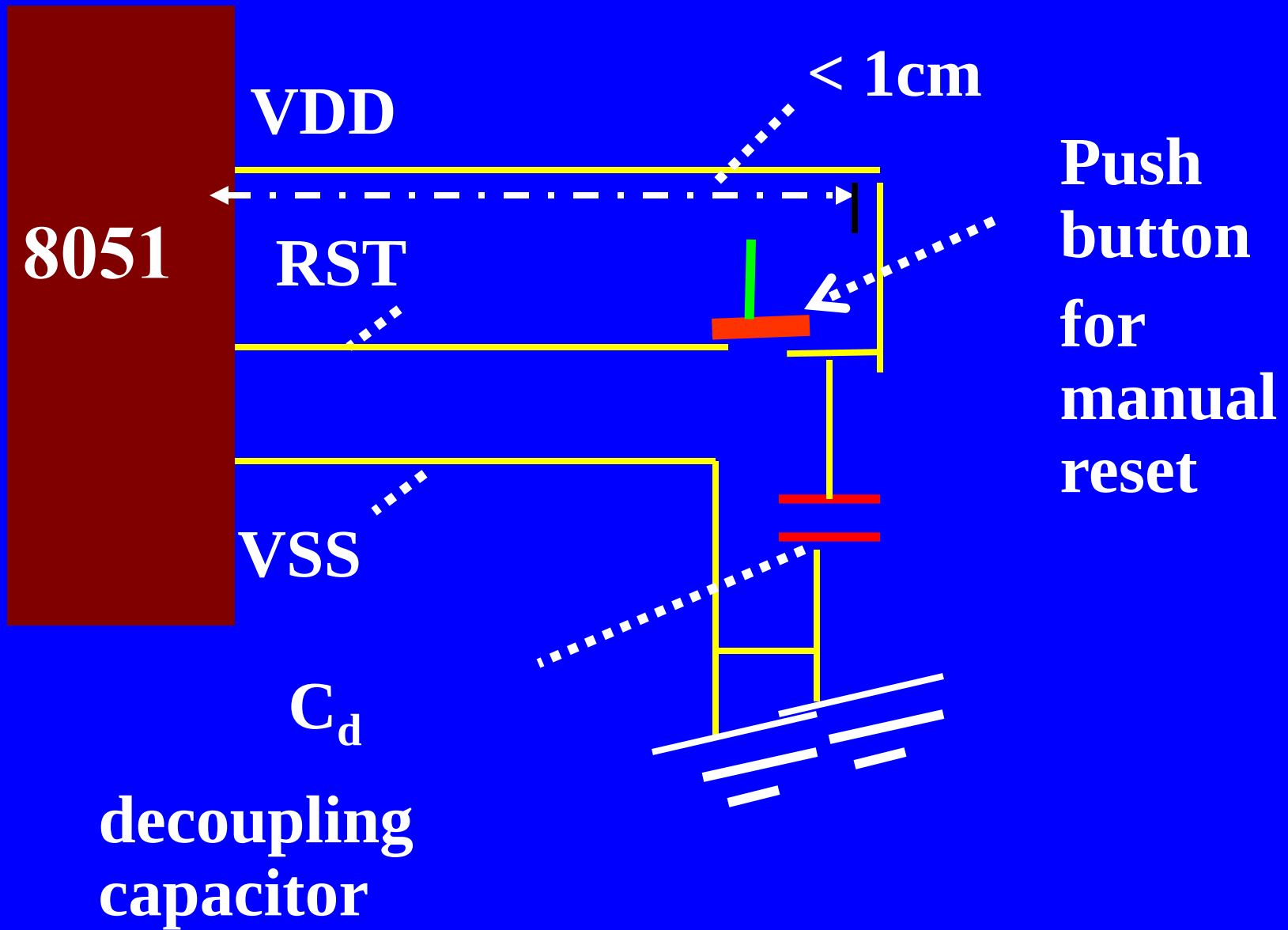
Supply circuit



Reset circuit

Internal Resistance




8051
VDD
< 1cm
RST
VSS
C_d
decoupling capacitor
Push button for manual reset

Summary

We learnt

- 8051 family 8-bit processor
- PC, SP, PSW
- Harvard architecture
- 8 bit data types
- Little endian 16-bit word alignment
- Interrupts – Maskable Interrupt requests (INT0, INT1)
- PC 0000H at reset

We learnt

- Internal SFR Addresses- IO/Devices Control and Status SFRs, SP
- Internal RAM Addresses
- Internal and External ROM addresses
- External RAM addresses

We learnt

Internal Devices

- T0 and T1
- SI
- WDT

We learnt

Pins

- Port P0 with option of AD0-AD7
- Port P1
- Port P2 with option of AD8-AD15,
- Port P3 with options WR, RD, T1, T0, INT1/GT1, INT0/GT0, TxD/CLK, RxD/Data

We learnt

Pins

- VDD and VSS
- XTAL1and XTAL2
- EA, ALE, PSEN, RST