

Chapter 2

Overview of Architecture and Microcontroller-Resources

Lesson 1

Additional resources to a microprocessor in Microcontroller Architecture

Port P2

Port P3

Port P1

Port P0

Timer

SFRs

Data Memory
64B

Program
Memory 1 kB

CPU

RAM

ROM,
EPROM
or FLASH

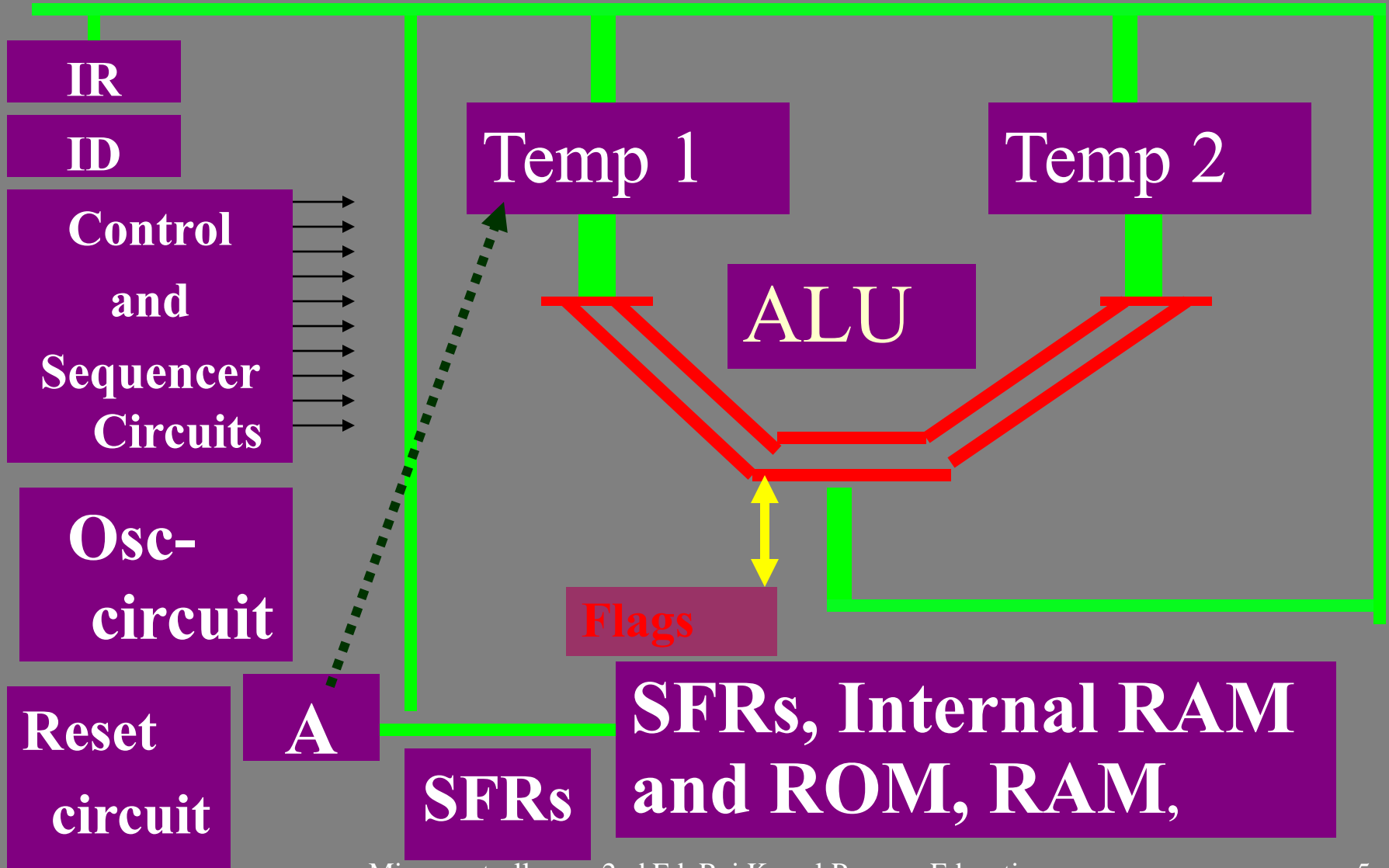
Microprocessor
resources

8048 MCU (CPU + Internal Resources)

Pointer 16-bit Registers

- 16-bit Program Counter PC to point to program memory
- 16-bit Data Pointer DPTR points to external data memory.
- DPTR—two bytes DPH-DPL (two SFRs)

8048 Execution Unit



- Instructions have operands of **8-bit** data type

Internal bus

Fetch

IR

Decode

ID

Execution

Control
and
Sequencer
Circuits



Control memory

Micro codes based -Implementation

Buses and XTAL

- 16-bit and 8-bit internal buses separate for program memory and data memory
- 16 bit address and 8 bits external data buses to program and data memory
- XTAL- Osc circuit

8051 Family Boolean Processing Unit

- An additional Boolean Processor for the operations on single bits
- Bit transfer, Bit XOR, OR, AND, Complement Operations

8048 Architecture view

- Harvard architecture bus
- Bus interface for 16-bit/8-bit address, data and instructions.
- 1 Interrupt requests INT at P3.2
- PC initialization 0000H

Reset



Port P1

Port P2

Port P3

Timer

Port P0

**Internal
Program
Memory**

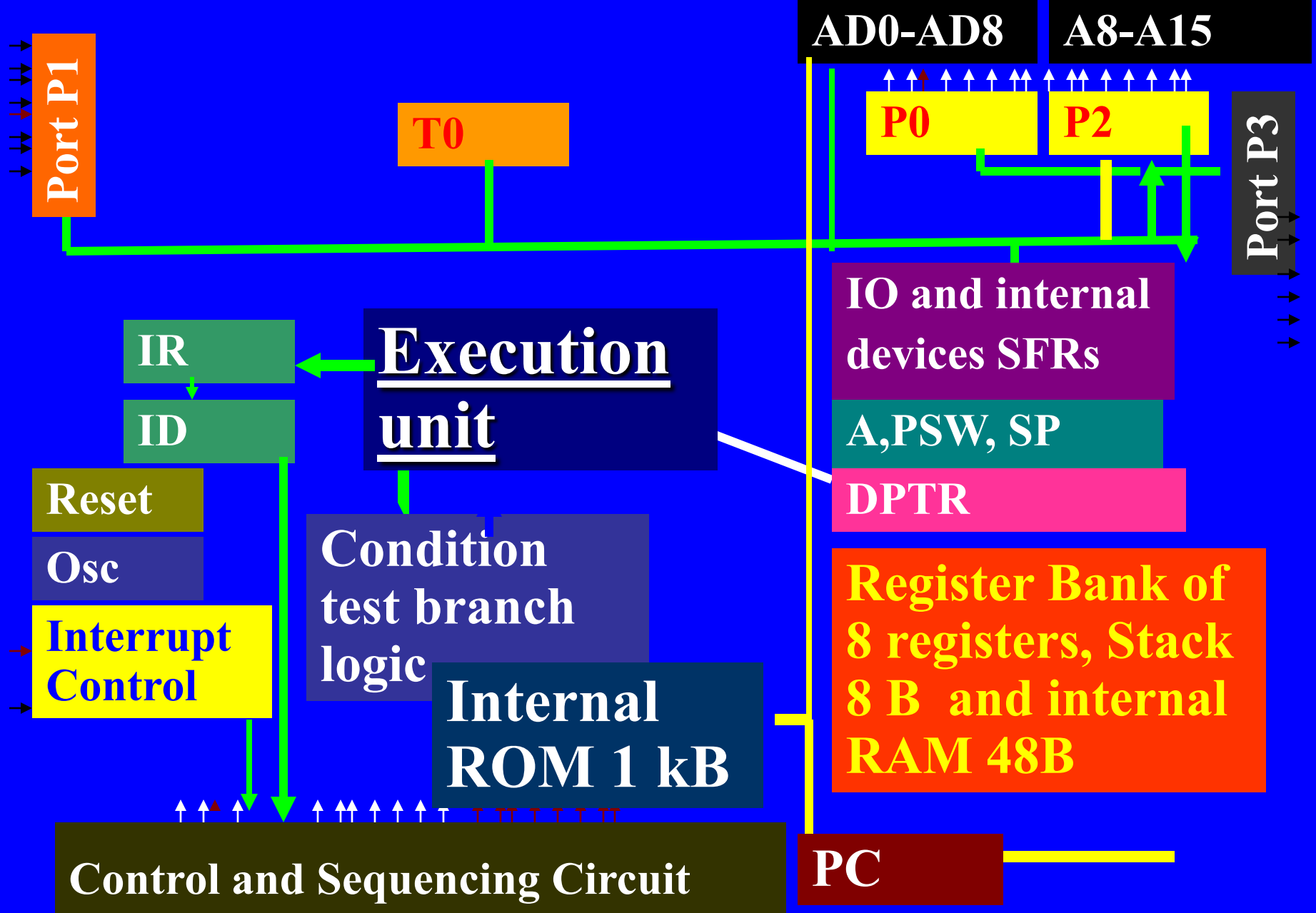
**Internal
Data
Memory**

**ROM,
EPROM**

**8048 on-chip
Resources**

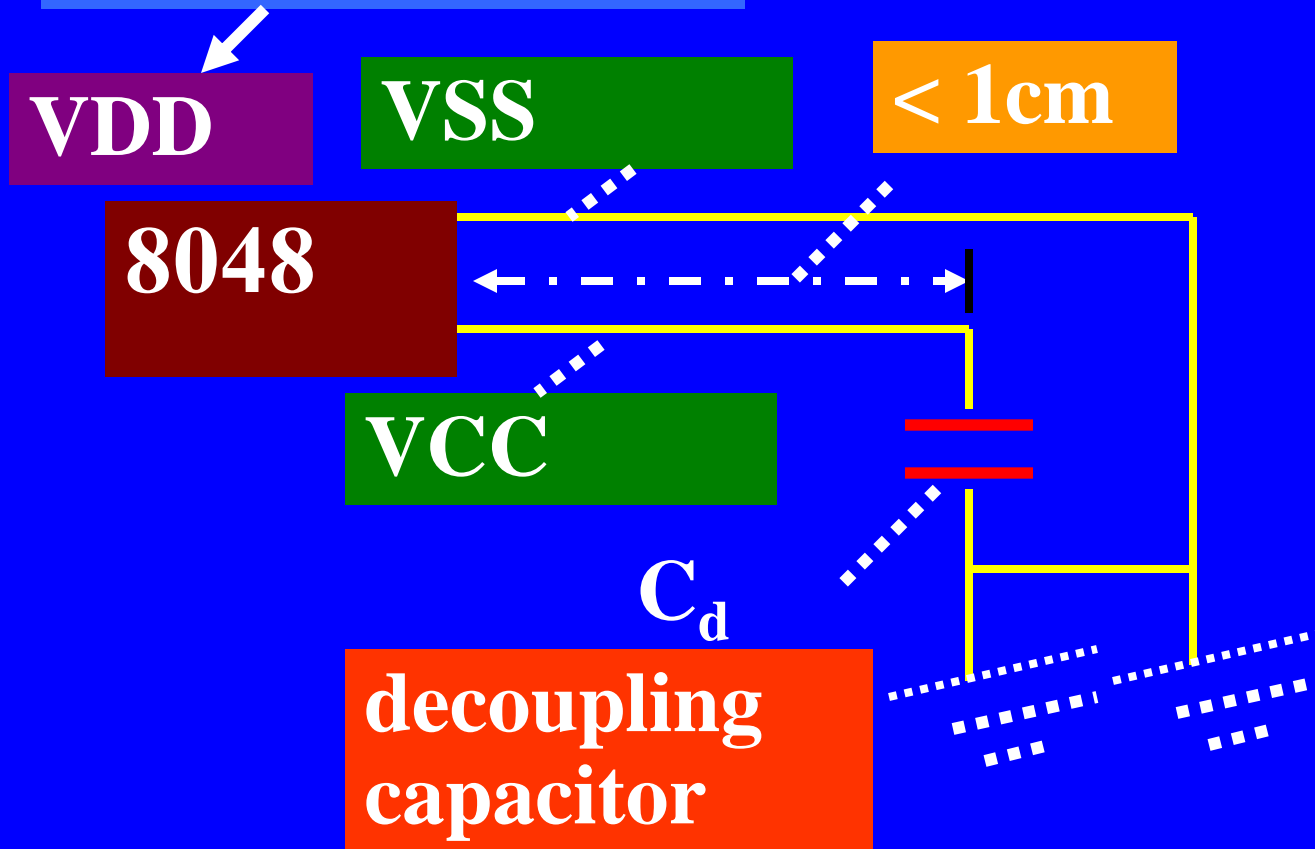
RAM

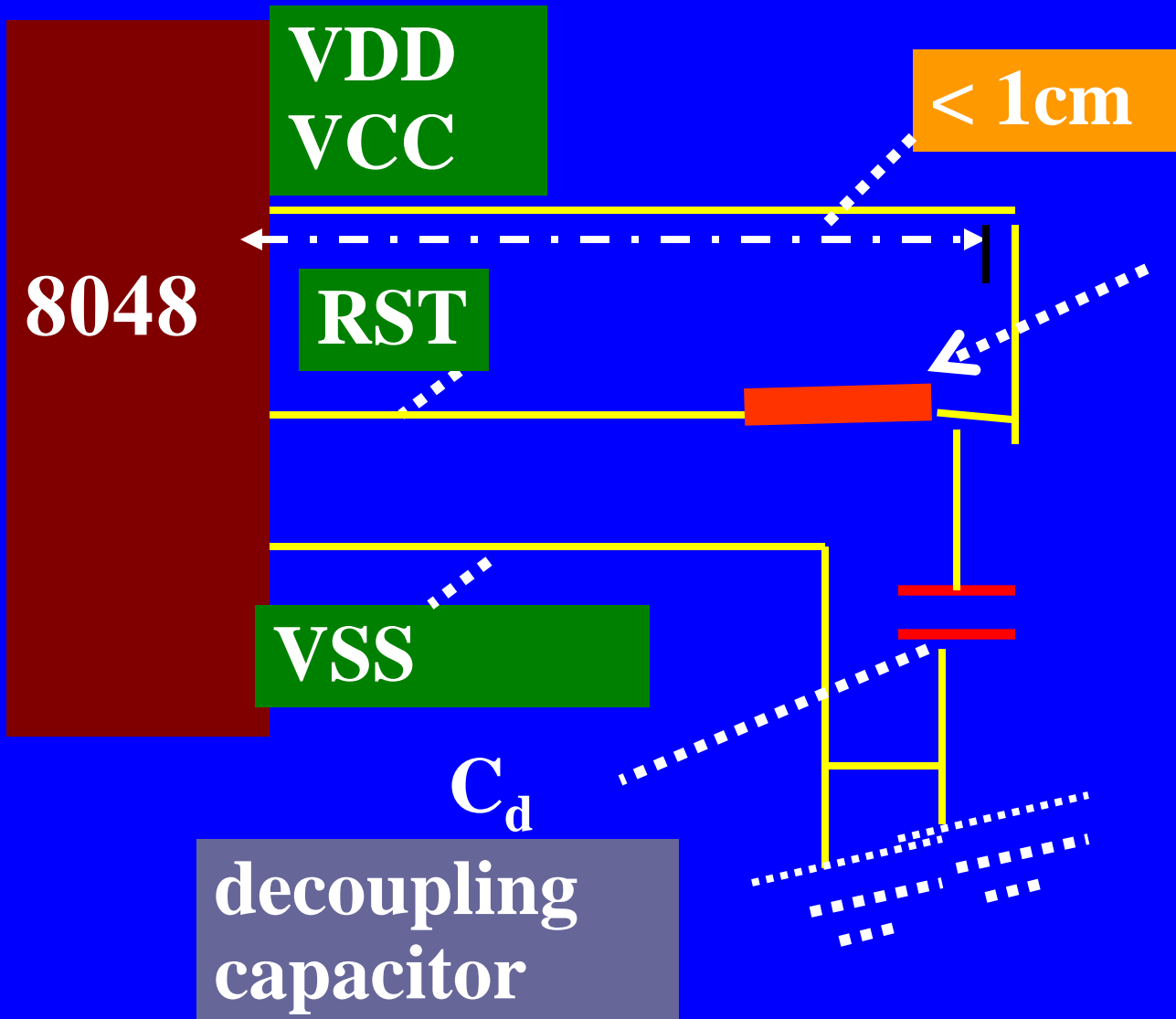
Microcontroller-resources



Supply circuit

Standby power

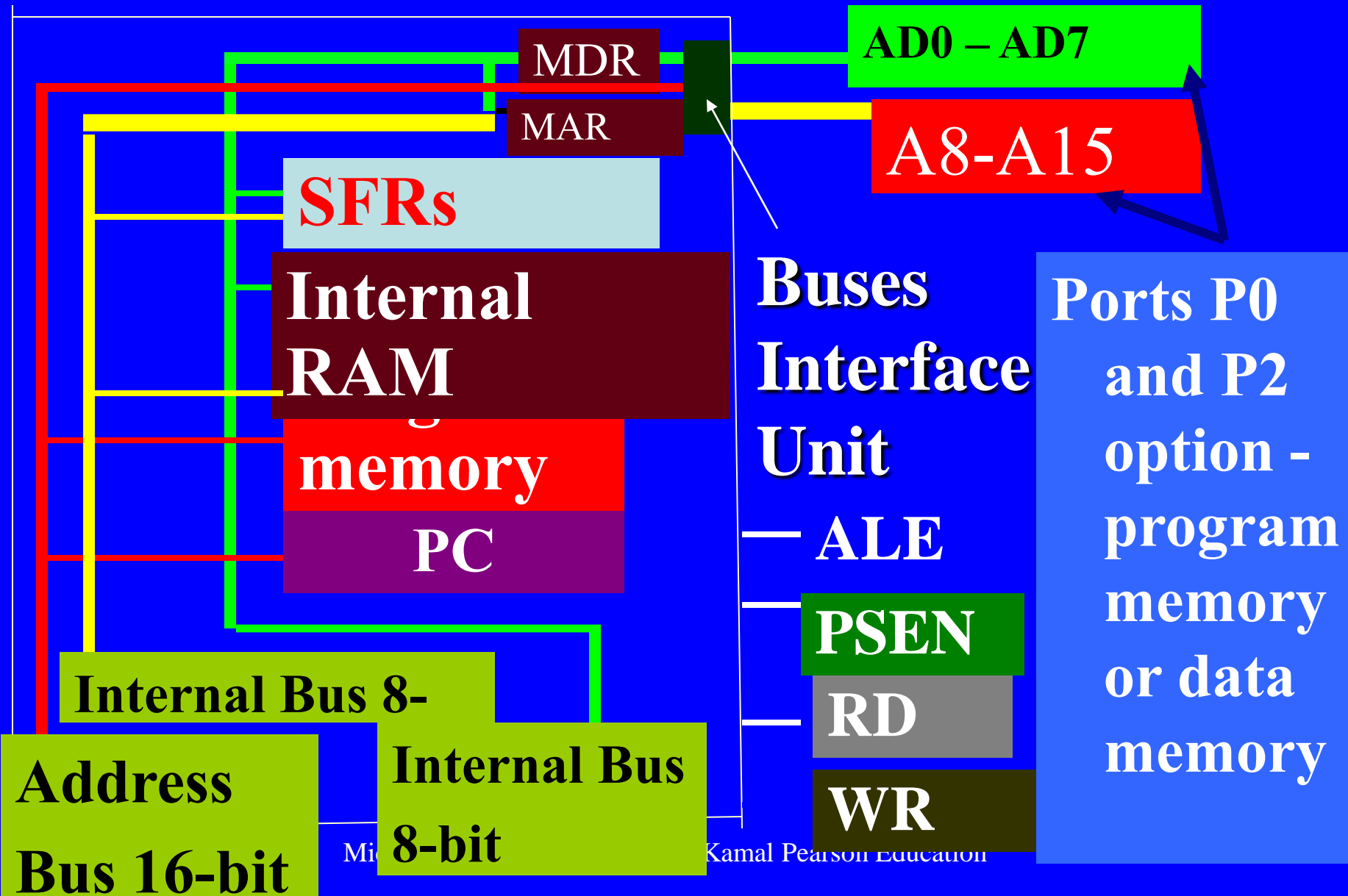




An IC for reset or a Push button for manual reset

Reset circuit

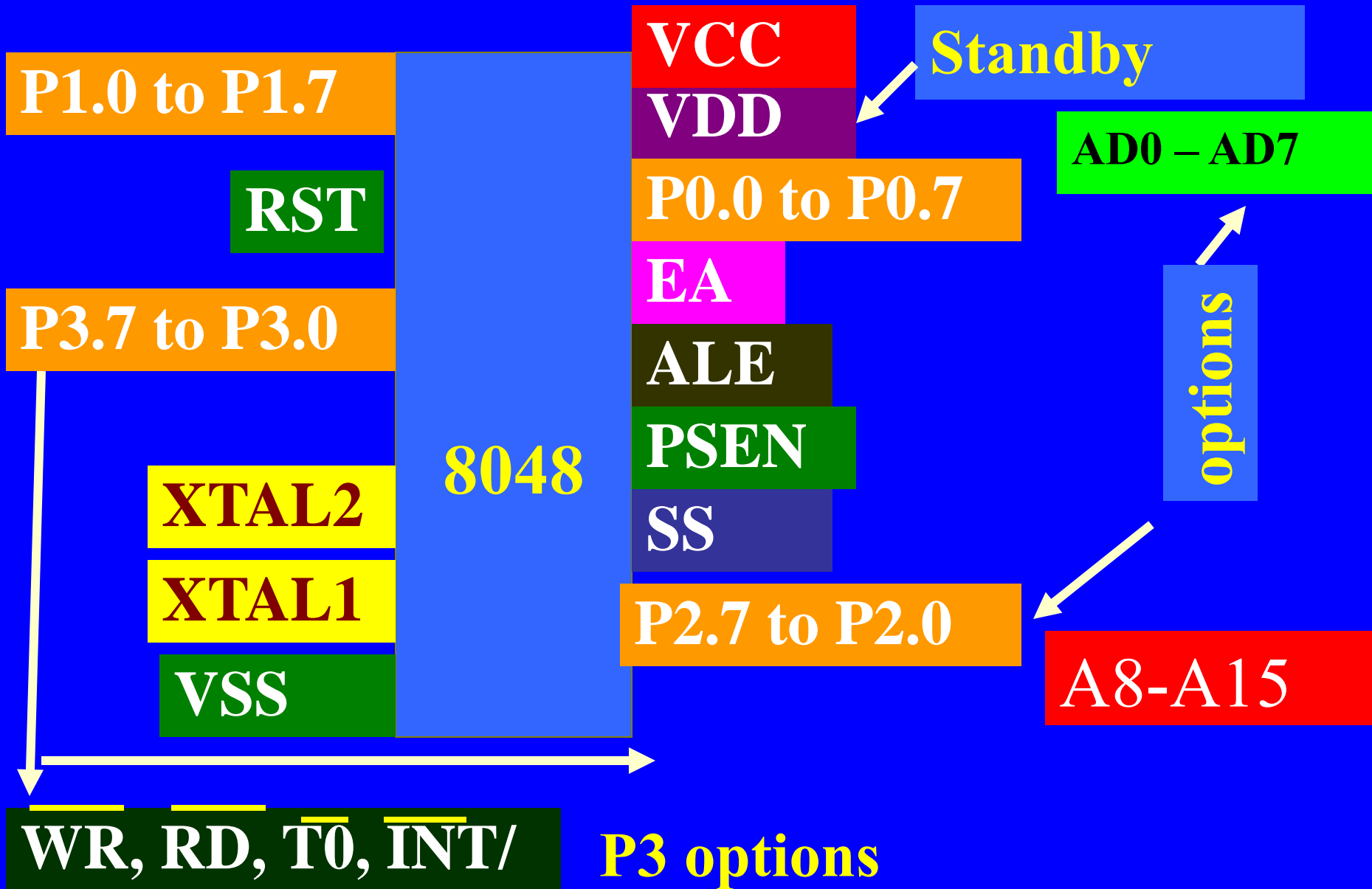
Internal and External Buses



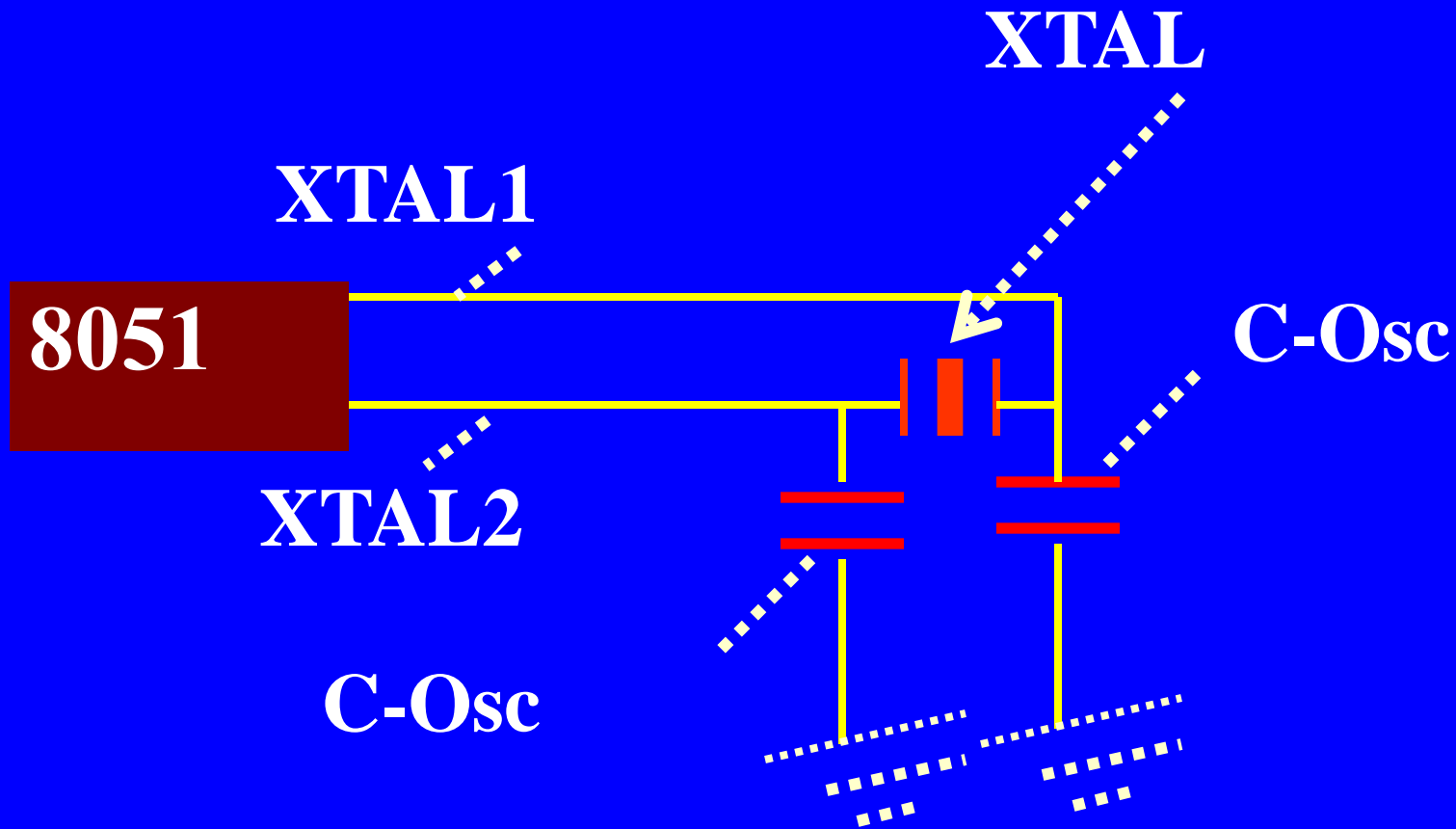
Internal Device

- Timers T0 - Event Counter

8048 Pins



Oscillator Circuit,



$\overline{\text{EA}}$, ALE , $\overline{\text{PSEN}}$, $\overline{\text{SS}}$

- $\overline{\text{SS}}$ means single step mode
- $\overline{\text{EA}}$ is made 0 by user to enable use of external program memory space in place of the internal program memory space
- Control signal $\text{ALE} = 1$ to enable latching of address A0-A7 bits from AD0-AD7
- Control signal $\overline{\text{PSEN}} = 0$ to enable read of program memory bits from external program memory

Outline

- 8048 MCU Feature and Resources
- Execution Unit- ALU
- MCU Architecture overview
- **8051 Series Family Members**
- 68HC11 Series Family Members

8051 Series Family Members

**64 kB
Data
RAM**

**64 kB
Program
Memory**

**8051
Classic**

**8051
Extended**

**Philips
8051 MX**

**4 kB ROM,
128 B RAM
Internal**

8051 Series

8051 Series Family Members

**4 kB ROM,
256 B RAM
Internal**

**Extended 16
MB Data
RAM**

**Extended
16 MB
Program
Memory**

**8051
Classic**

**8051
Extended**

**Philips
8051 MX**

8051 Series

8051 Series Family Members

**External/
Internal
unified**

**8 MB ROM
+ 8MB
Constants
ROM**

**Unified 64 MB
Program/Data
Memory**

**8051
Classic**

**8051
Extended**

**Philips
8051 MX**

8051 Series

**16-bit Stack
Pointer,
768 B
Internal
RAM**

68HC11/12/16 Series Family Members

**Internal/External Unified 64 kB
Data RAM/ Program
memory/EEPROM**

8-bit MCU

68HC11

68HC12

68HC16

4 Ports

68HC11/12/16

Series

68HC11/12/16 Series Family Members

**Internal/External
Unified 4 MB Data
RAM/ Program
memory/ EEPROM**

8CH. Timers

**16-bit
PACNT**

16-bit MCU

12 Ports

68HC11

68HC12

68HC16

68HC11/12/16
Series

68HC11/12/16 Series Family Members

Enhanced 68HC12

Advanced Timers, ADCs

**16-bit
PACNT**

16-bit MCU

16 Ports

68HC11

68HC12

68HC16

68HC11/12/16

Series

Summary

We learnt

- Microcontrollers— A CPU with on-chip Ports, Memory, Special Function Registers, timers and other registers

We learnt

- 8048/51 family 8-bit processor, Harvard architecture
- 8051 has Boolean processing unit also
- 68HC11/12/16 Series, Princeton Architecture