# Chapter 12: Multiprocessor Architectures

Lesson 11:

**Hardware synchronization mechanisms**

# Objective

- **To understand the hardware based synchronization mechanism**

# Hardware Synchronization protocols

# Hardware Synchronization mechanisms

- Hardware cache coherence maintained in the systems such as Sun Enterprise 5000
- Higher speeds possible using cache controller, which has hardware for snooping

# Hardware Synchronization mechanisms

- The controller snoops through transactions over the bus
- A processor for hardware synchronization can have cache snooping circuitry with signals for other processors— snoop read hit and snoop write hit

# Hardware Synchronization mechanisms

- Hardware handles the implementation
- Complications for cache coherence due to write races

# Write Race Problem

- Write race means that the cache cannot update till the bus is available and the other processor gets the bus and does the write to the same cache line

# Two sequential processes for Hardware synchronization

- By bus arbitration and place appropriate signals for the cache miss
- A bus that splits the transactions
- There can be multiple transactions on split sections

# Hardware synchronization methods

- Use of semaphores
- Asynchronous signaling by busy and interrupt logic
- Synchronous transfers with collision detection

# Summary

# We Learnt

- Hardware synchronization and methods

End of Lesson 11 on

**Hardware synchronization mechanisms**