Chapter 12: Multiprocessor Architectures

Lesson 08:

Bus Shared Memory Systems

Objective

- To understand bus shared memory systems

Bus sharing

Bus sharing in memory architecture

- Bus request and grant mechanisms
- Processor or controller gets access to the bus at any given instance as a bus master
- The interprocessor network may be such that it simply acts as a medium for communication

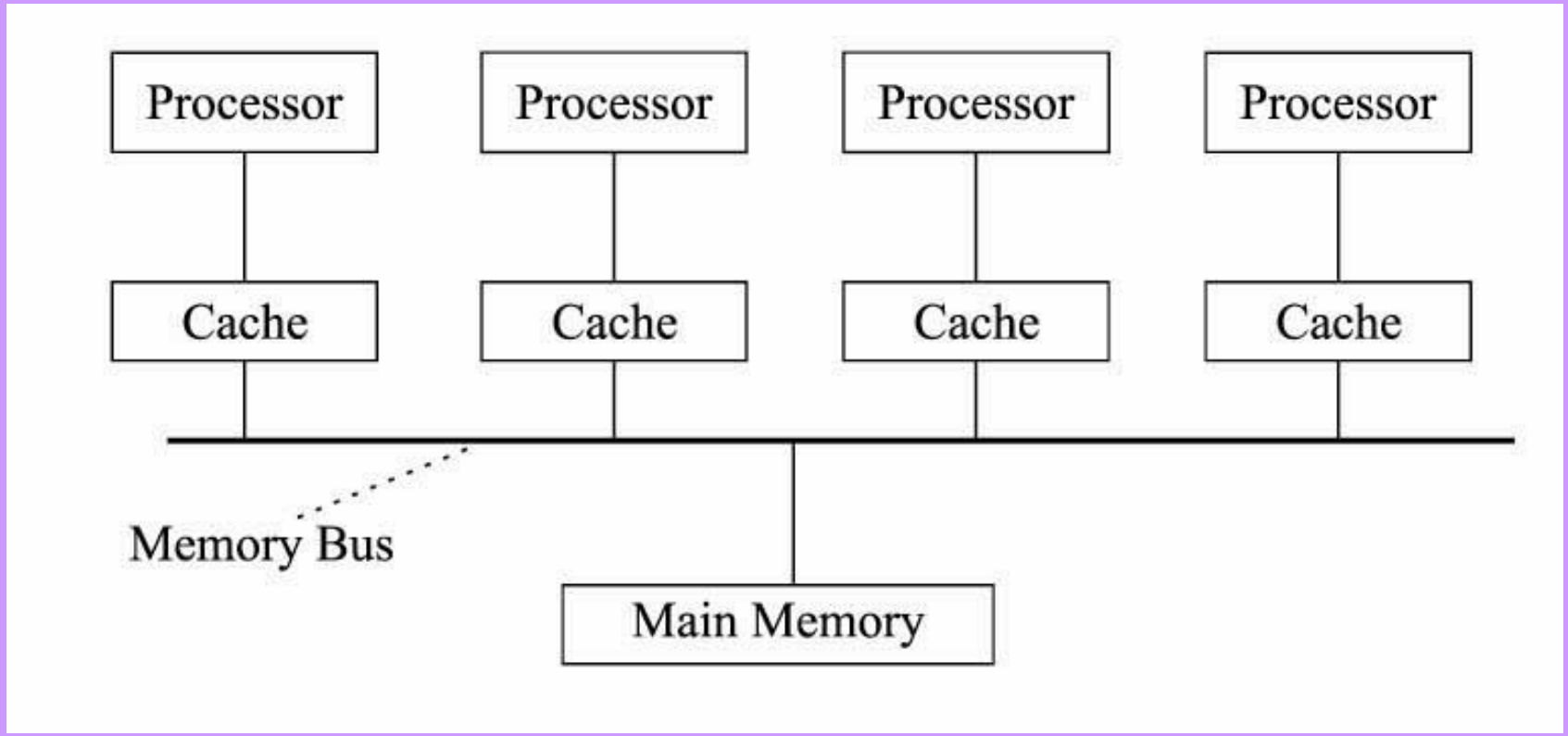
Bus sharing in memory architecture

- Bus─ more than a simple communication system
- Bus─ follows certain protocol-based signals and sequences to ensures that only one processor is able to function as a master of the interconnection bus at an instance

Bus sharing

- A common design for shared-memory systems—bus-based system
- Bus used as the communication network that connects the processors to each other and the centralized memory system

Bus sharing Architecture



Bus sharing

- Bus allows a variable number of processors to communicate with each other without changing the hardware
- Bus makes it easy to maintain cache coherence

Problem with more than one copy in the caches

- More than one cache may have a copy of a given memory location, creating the some cache coherence problem

Maintaining cache coherence using cache snooping

- In a bus-based multiprocessor easy because each processor in the system can observe the state of the memory bus, called cache snooping
- Cache snooping allow each processor to see any requests that other processors make to the main memory

Memory references on a bus shared-memory system faster completion

- When one processor makes a memory reference to an address that is contained in another processor's cache, the other processor can see the request, respond with the required data, and modify the state of its copy appropriately without ever involving the main memory
- Faster when some other processor has a copy of the required line compared to when the line has to be read from the main memory

Summary

We Learnt

- Bus shared memory system
- Allowing a variable number of processors to communicate with each other without changing the hardware
- Making it easy to maintain cache coherence

End of Lesson 08 on

Bus Shared Memory Systems