Chapter 12: Multiprocessor Architectures

Lesson 04:

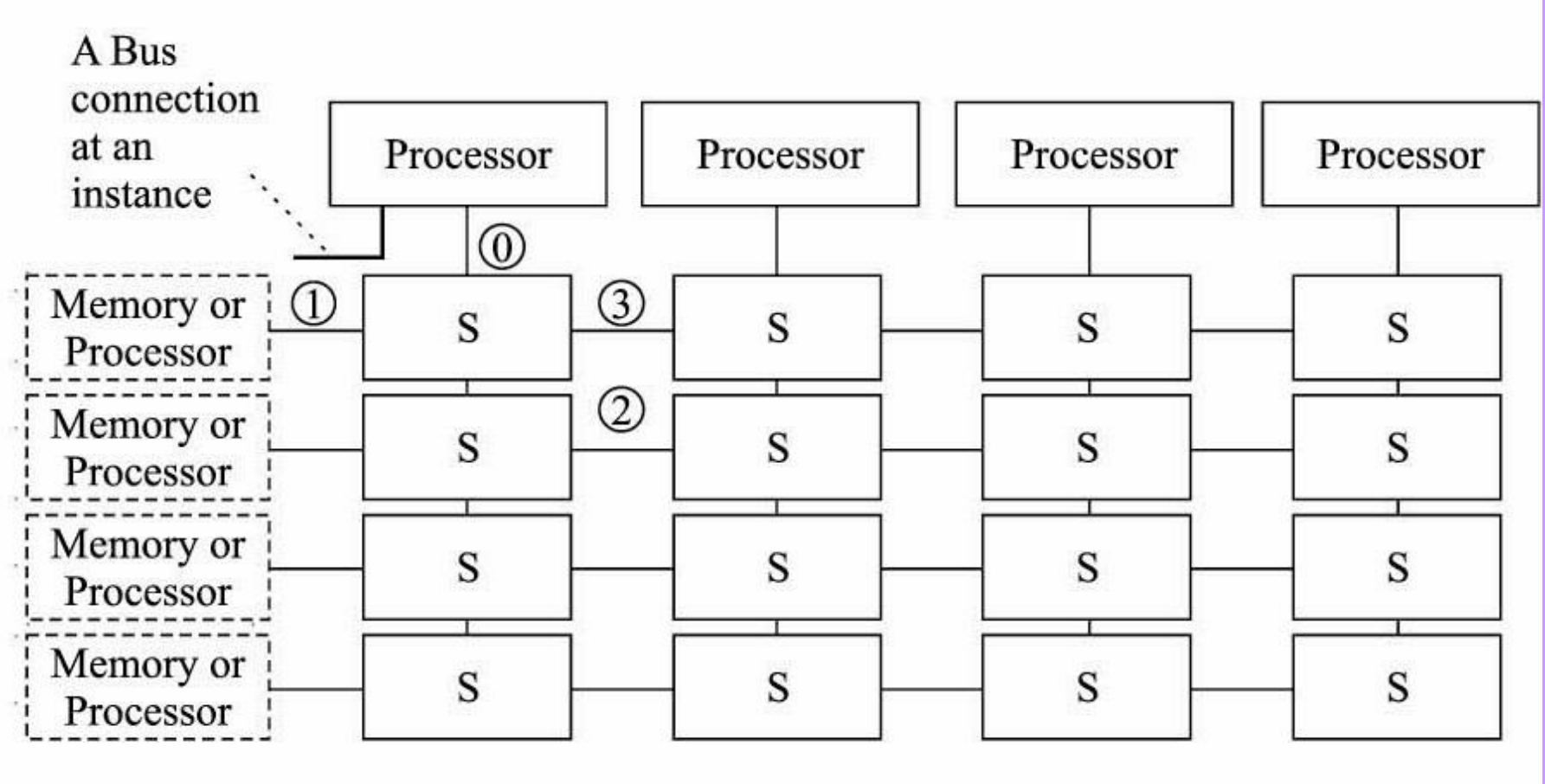
Interconnect Networks

Objective

- To understand different interconnect networks
- To learn crossbar switch, hypercube, multistage and combining networks

Crossbar Switches (Matrix Switch) for dynamic interconnections

Crossbar switch

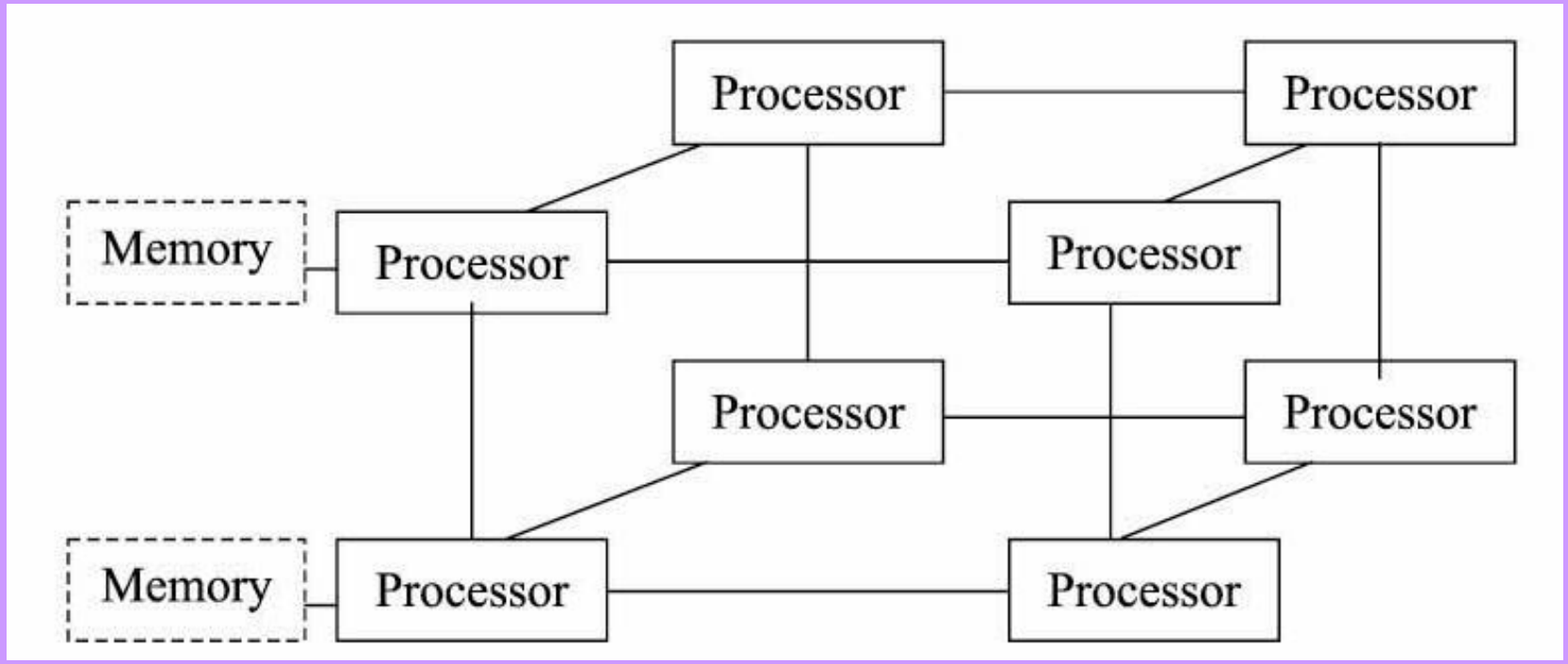


Crossbar switches for dynamic interconnections

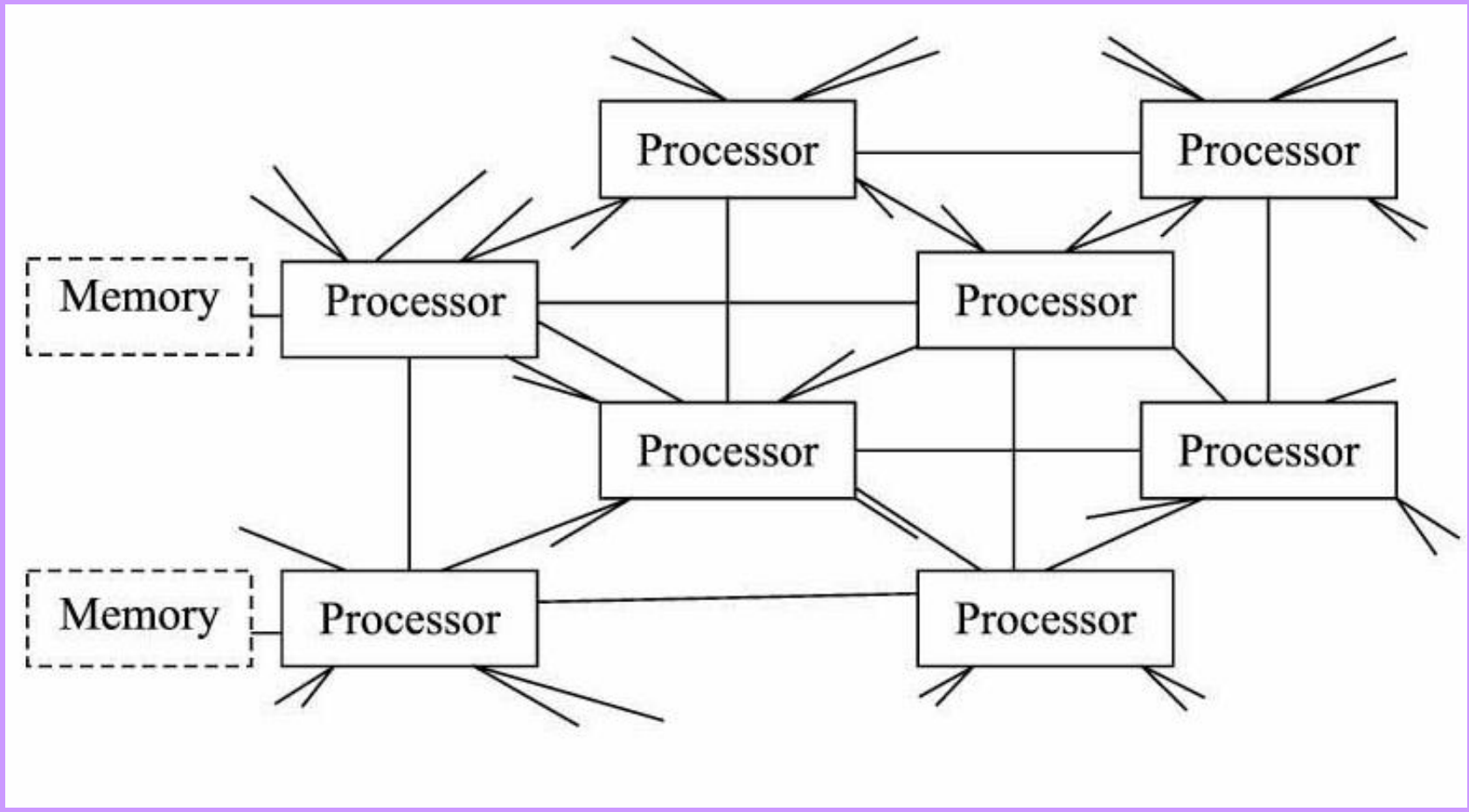
- Each processor has switch to memory bus horizontally and processor-to-switch links vertically
- A switch S having four I/O paths (0, 1, 2, 3) provides the following twelve paths (assume even paths horizontal, odd paths vertical): 0-2, 0-1, 0-3, 1-0, 1-2 1-3, 2-0, 2-1, 2-3, 3-0, 3-1, 3-2

Hypercube Networks

Hypercube (3-cube) networks

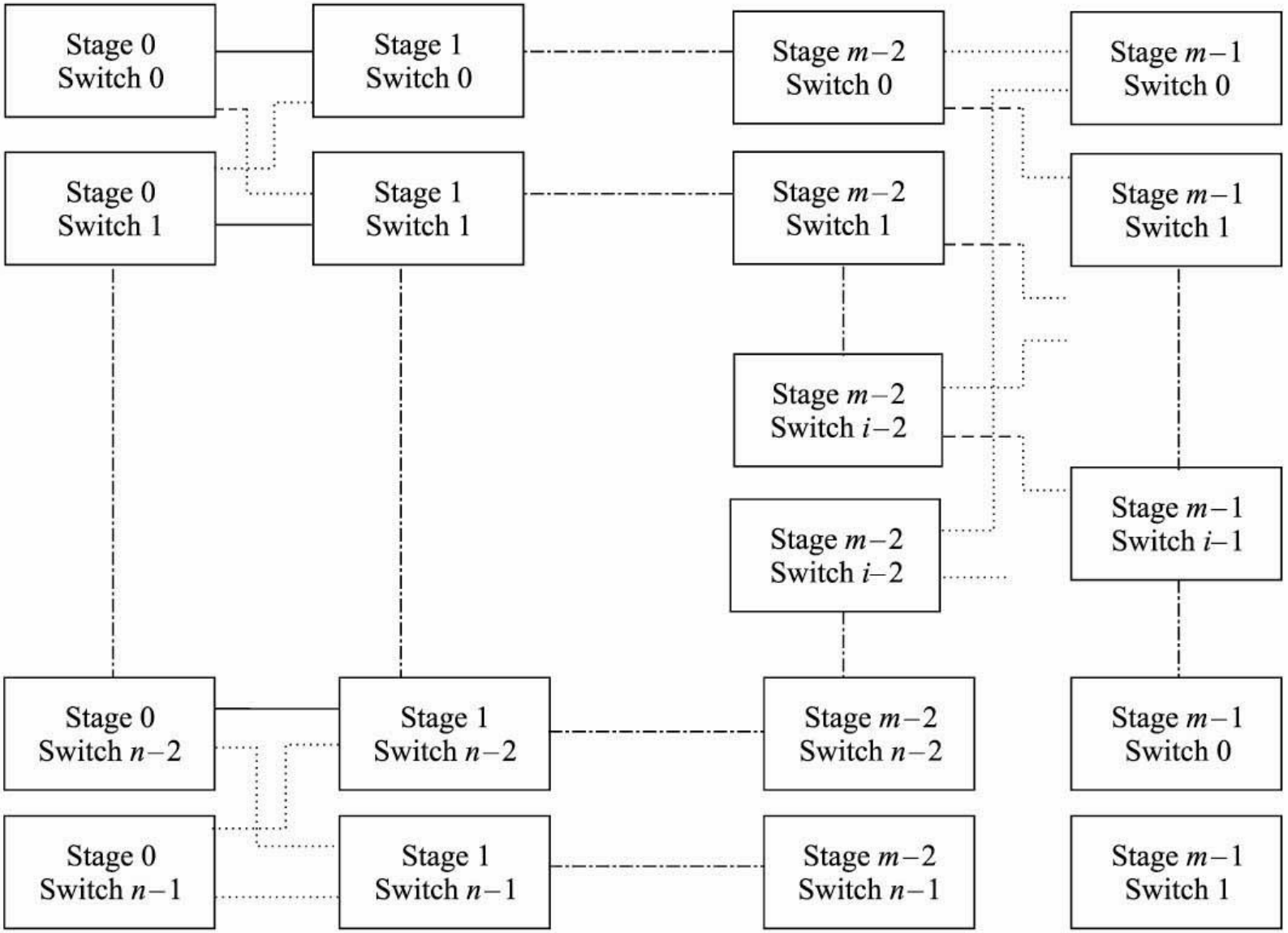


Hypercube (n-cube) networks



Multistage Networks

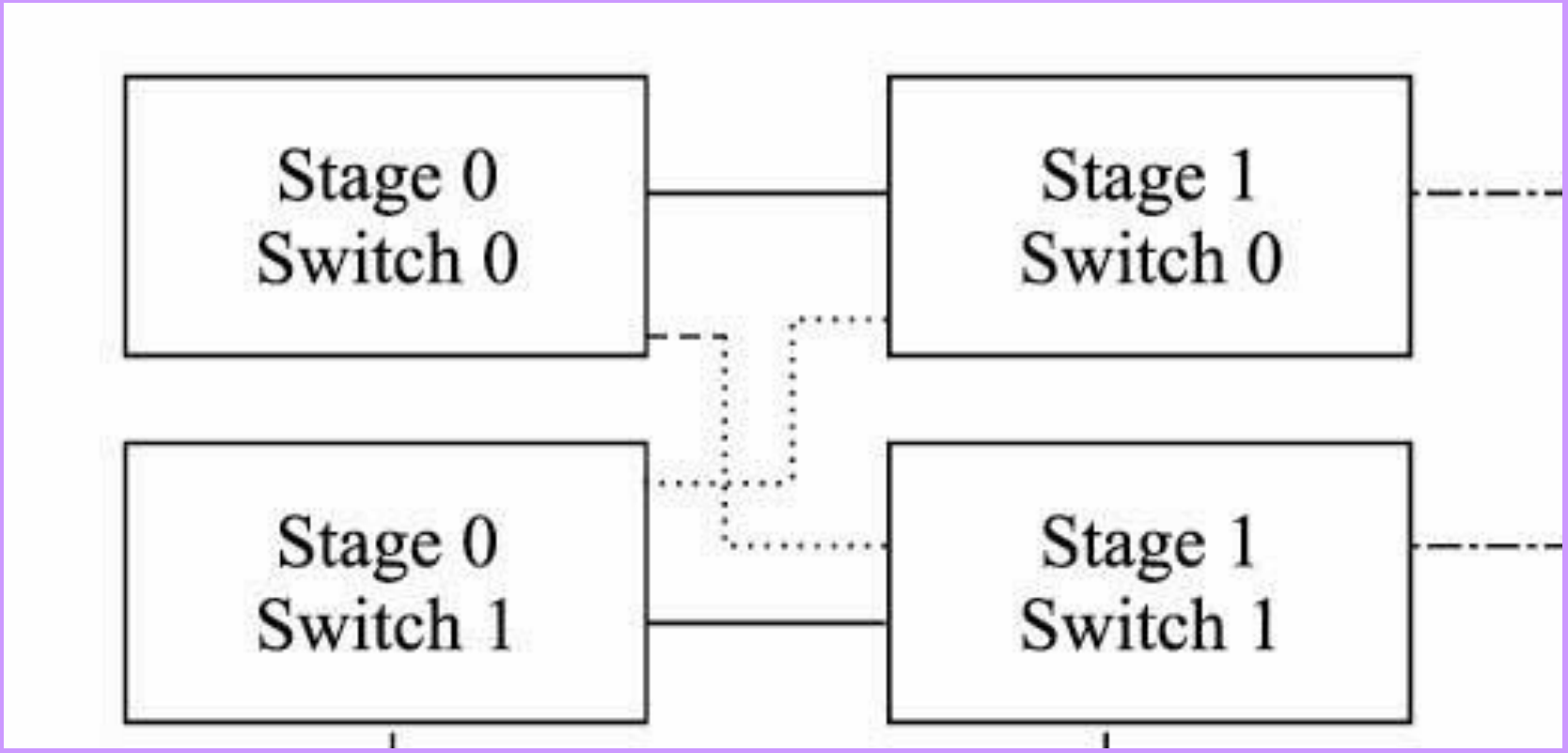
Multistage (Butterfly) network
m stage *n* switches multistage



Butterfly connection

- The 0^{th} output of stage j switch k connects to 1^{st} input of stage j +1 switch k–1 and 1^{st}t output of stage j switch k–1 connects to 0^{th} input of stage j + 1 switch k

Multistage (Butterfly) connection at 0^{th} stage



Butterfly and Shuffle connections in Banyan-Delta Networks

Multistage Network

- Banyan network
- *m* stage *n* switches multistage network example with butterfly and shuffle connections

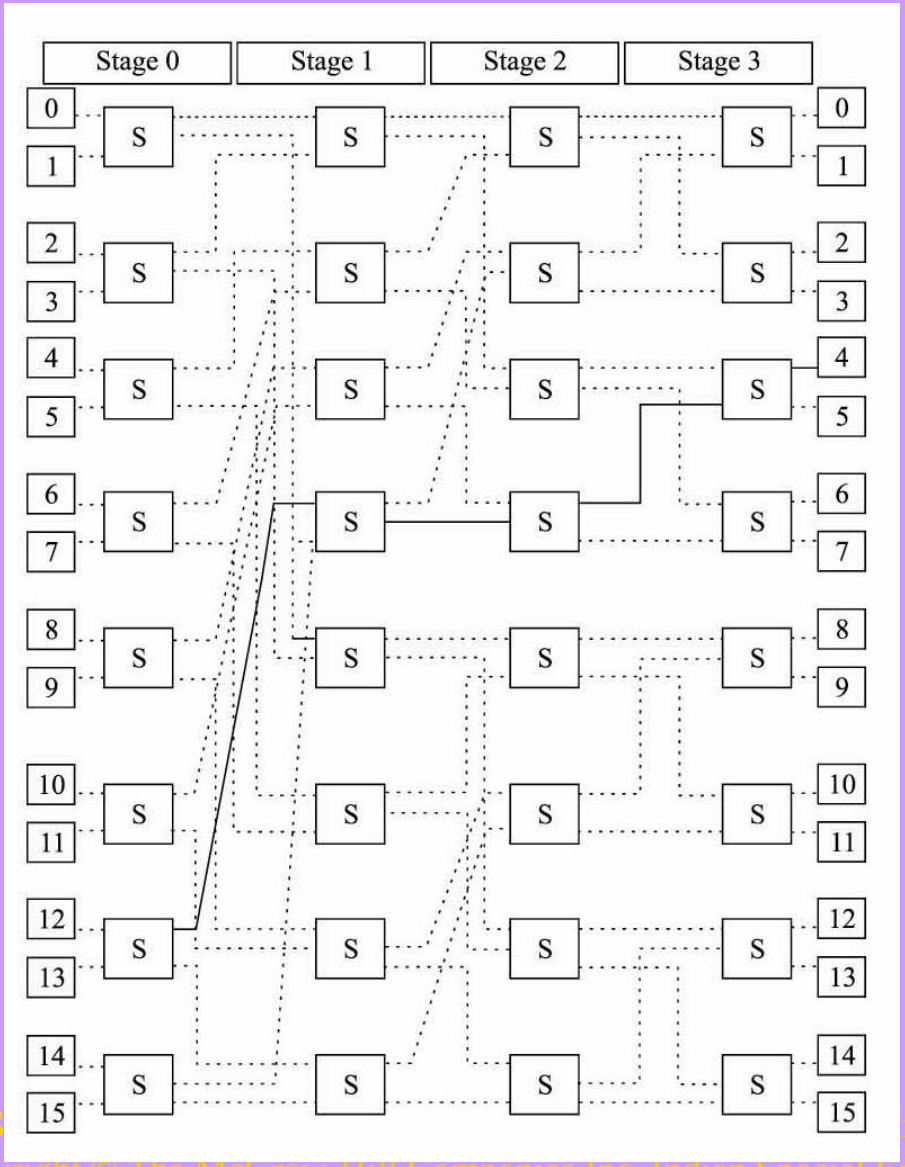
Butterfly and Shuffle connections in Banyan-Delta Networks

- Butterfly help in one switch up or down, when the route path changes from stage j to $j + 1$
- One switch up or down, when the route path changes from stage j to $j + 1$

Butterfly and Shuffle connections in Banyan-Delta Networks

- Shuffle helps the 1^{st} output of stage j switch k connects to 0^{th} input of stage j +1 switch $k + i$ and 0^{th} output of stage j switch $k + i$ –1 connects to 1^{st} input of stage $j + 1$ switch k

Multistage (Butterfly) and Shuffle connections at the stages

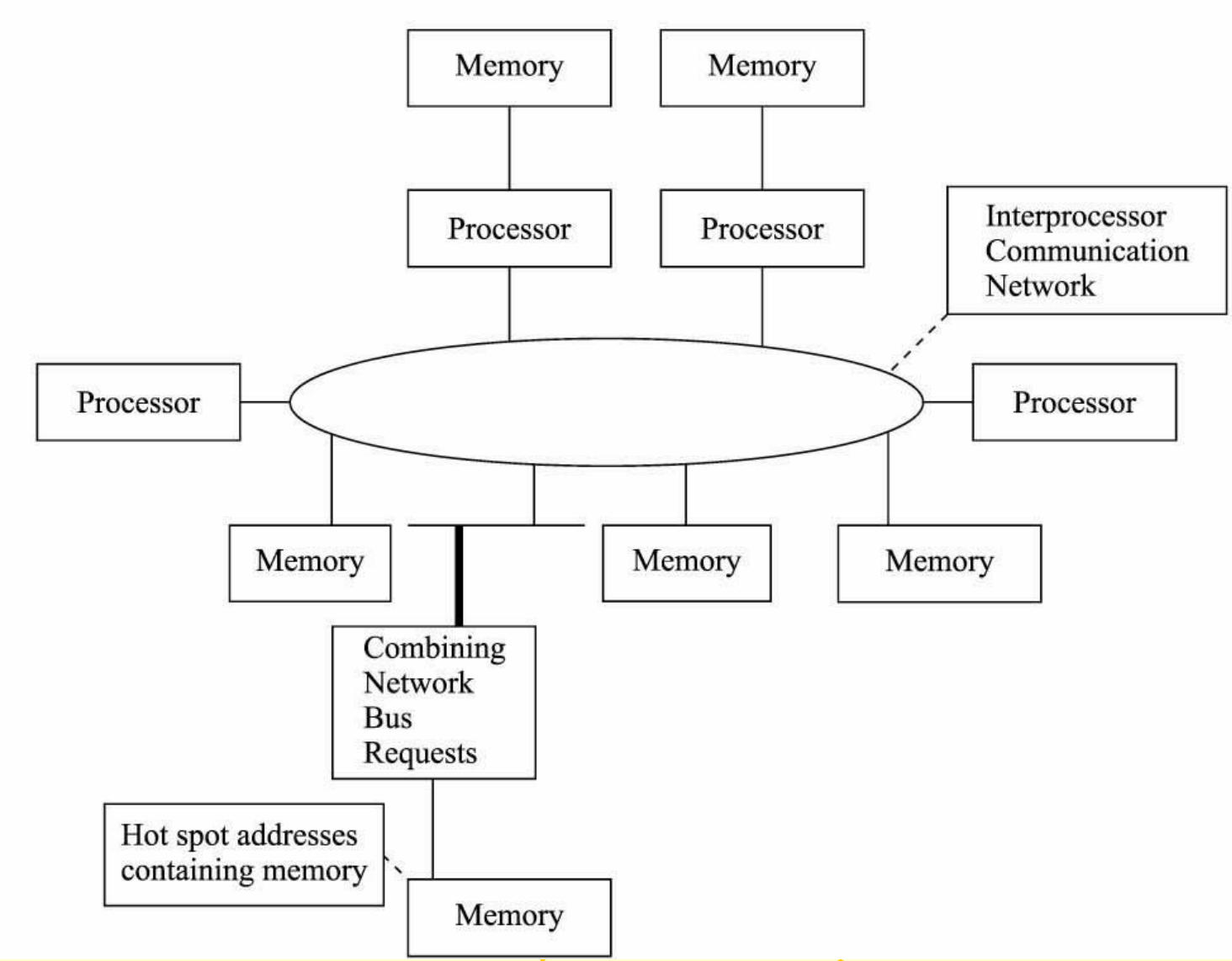


Banyan Network Connections table for 4 × 14 stages

Stages 0-1	0-0	1-8	3-9	5-10	7-11	9-12	11-13	13-14
	2-1	4-2	6-3	8-4	10-5	12-6 ✓	14-7	15-15
Stages 1-2	0-0	1-4	3-5	5-6	7-7 ✓	9-12	11-13	13-14
	2-1	4-2	6-3	8-8	10-9	12-10	14-11	15-15
Stages 2-3	0-0	1-2	3-3	5-6	7-7	9-10	11-11	13-14
	2-1	4-4	6-5 ✓	8-8	10-9	12-12	14-13	15-15

Combining in Networks

Combining network bus requests



Summary

We Learnt

- Crossbar switch interconnects for multiprocessor networks
- Hypercube interconnects
- Multistage interconnects
- Combining the interconnect network memory requests

End of Lesson 04 on

Interconnect Networks