Chapter 12: Multiprocessor Architectures

Lesson 03:

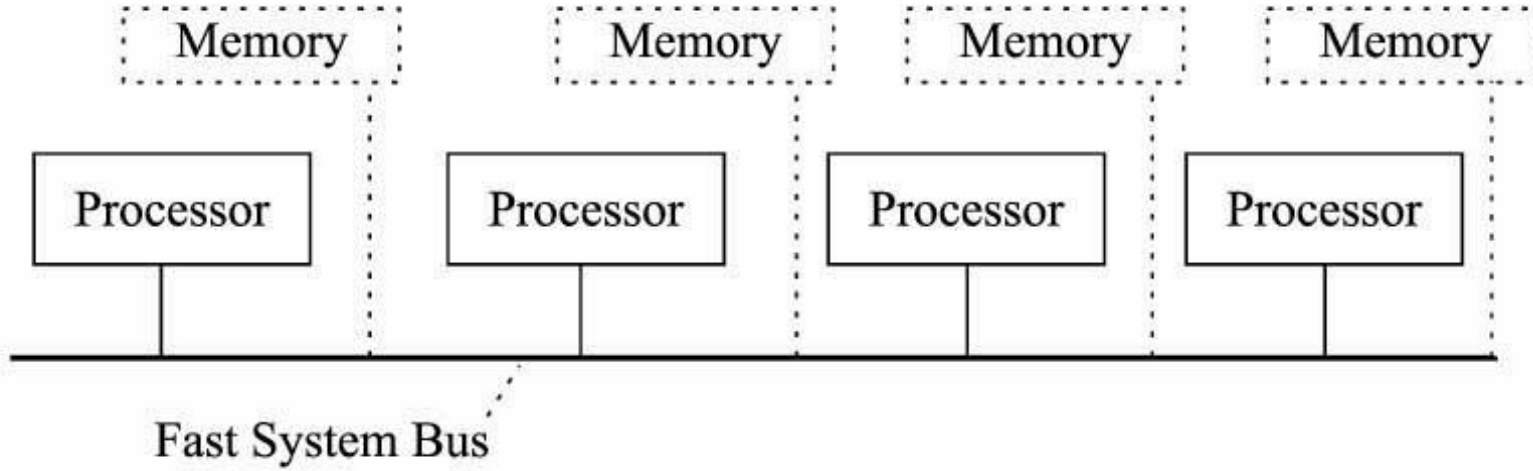
Multiprocessor System Interconnects– Hierarchical Bus and Time Shared bus Systems and multi-port memory

Objective

- To understand multiprocessor system interconnects using system, hierarchal and time shared buses
- Use of SEND and RECEIVE functions and multiport memories

Fast System-Bus based Inter-communication Network for Sequential and Parallel Processors

Simple Interconnection network between multiprocessors

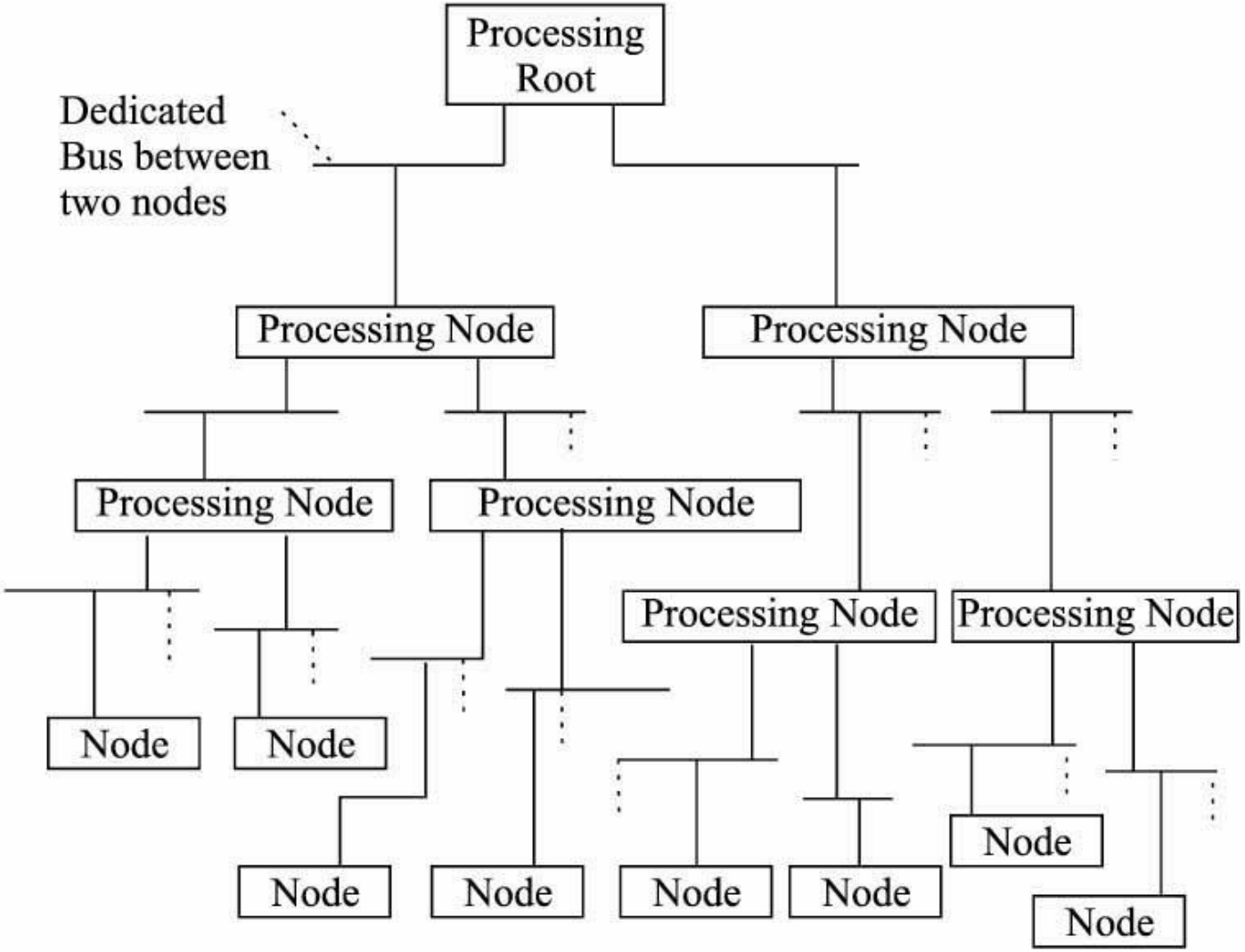


Simplest single network using a system-bus interconnection

- A contention problem when more than one processor seeks bus access at the same time
- Specialized design can solve the contention issue to large extent

Hierarchical Bus Systems for Sequential and Parallel Processors

Hierarchical Tree-like Design of the Processing Nodes with each Node having two dedicated interprocessor Buses



Buses in a hierarchical tree-like design of multiprocessors

- A root processor with two or more dedicated buses at each node
- Each node─ an independent processor and memory

Buses in a hierarchical tree-like design of multiprocessors

- Hierarchical design with two independent processing node buses

Buses in a hierarchical tree-like design of multiprocessors

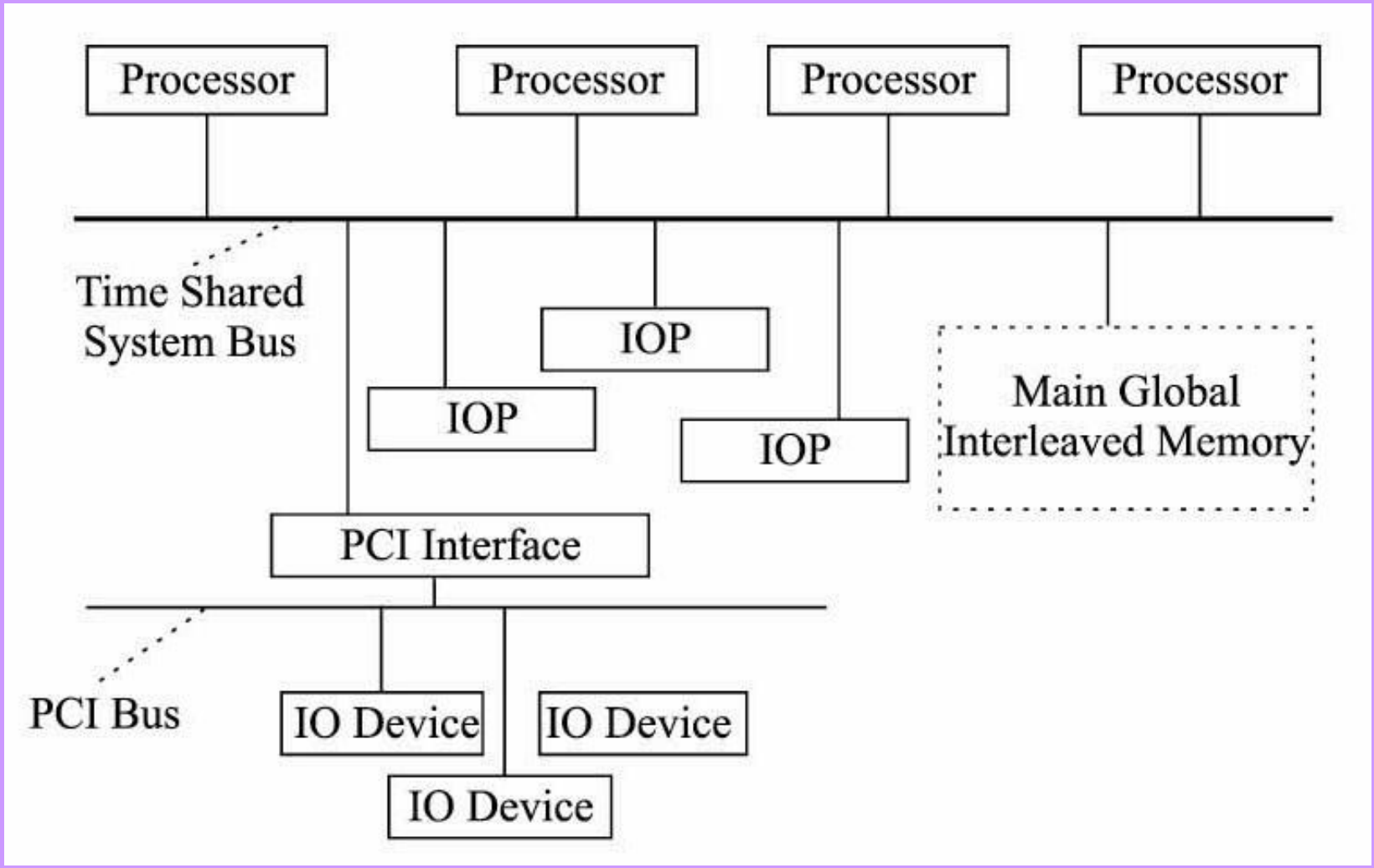
- Communication─ by message-passing
- Each processor node executes a RECEIVE (buffer) operation, wait till SEND not completed
- The sending processor executes its matching SEND (data, destination) operation before the RECEIVE operation executes

Buses in a hierarchical tree-like design of multiprocessors

- RECEIVE─ a wait operation for taking message when a processor node *A* raises the need to receive data
- SEND ─ message post operation by other processor node *B* presently using the bus
- The processor *A* gets the needed bus for receiving the data after the SEND

Time shared Bus Systems for Sequential and Parallel Processors

Time shared Bus Design of the Processing Nodes- PCI Bus Example



Example of Time-shared System Bus

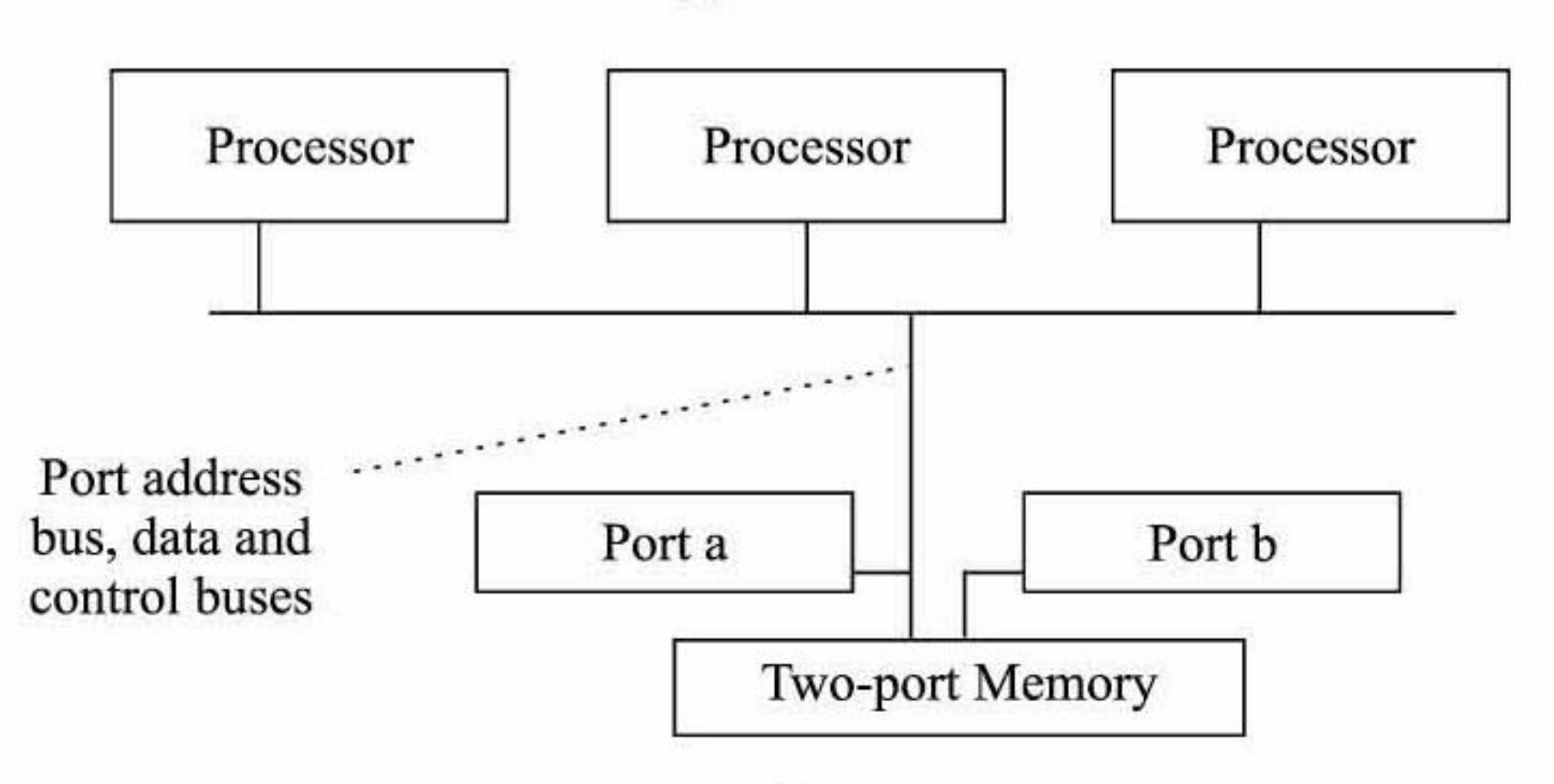
- System bus shares the time slots between Processors, Input-Output Processors (IOPs) and Connects to PCI Bus for I/O Devices

Use of Multiport Memories for Interconnections of simultaneous accesses by multiprocessor memories

Multiport Memory

- A multi port memory has the cells in which there are two or more ports where write can be made to one, while two or more ports can be simultaneously addressed and read

Multiport memory network



Multiport memory

- Supports simultaneous access, sometimes across different bus widths and voltages
- When it imposes no delay on either port during a read or write operation, then its maximum performance exceeds the traditional multiplexed SRAMs by a factor of at least two

Use of Synchronization mechanism in hardware in multi-port port memory

A hardware synchronization mechanism

- Solves the simultaneous access for read and writes to the same port

New synchronous dual-port memories

- Collision detection logic support
- Speeds up to 200 MHz
- Bandwidth up to 1.75GB/s achieved for the multiprocessor systems

Summary

We Learnt

- Simple system bus interconnect network
- Hierarchical Tree like bus interconnect network
- Time shared bus structure
- Use of RECEIVE and SEND functions for message passing from one processor to another
- Use of multiport memories for simultaneous accesses to the memory in a multiprocessor system

End of Lesson 03 on

Multiprocessor System Interconnects—Hierarchical Bus and Time Shared bus Systems and multi-port memory