Chapter 11: Input/Output Organisation

Lesson 15:

Standard I/O bus– PCI

Objective

- Familiar with I/O bus and standard I/O interfaces─ parallel bus PCI (Peripheral Connect Interface) for a synchronous parallel communication interface bus
- Learn that PCI has 32-bit data bus extendable to 64 bits, 32-bit addresses extendable to 64 bits and total 100 PCI Bus-signals
- Learn the unique feature of PCI bus─ its configuration address space

Standard I/O bus

Standard I/O bus

- Defines a protocol for how the devices may access the bus, when data may be sent, and so on
- One of the key elements of this is the arbitration policy that is used to decide which device may access the bus at a given time

PCI a standard I/O bus

Standard back-plane I/O bus PCI

- Found in many PCs and workstations
- Provides a specification for how commands and data are transferred between the processor and the I/O devices
- How multiple devices compete for use of the bus

PCI

- Provides a synchronous parallel communication interface bus
- 32-bit data bus extendable to 64 bits
- 32-bit addresses extendable to 64 bits
- Its clock rate is nearest to the sub-multiple of the system clock

PCI

- An exemplary PCI Card has a 16 MB Flash ROM and a router/gateway for a LAN
- A PCI driver can access the hardware automatically as well as by the programmer assigned addresses

The PCI feature

- Automatically detection of the interfacing systems for assigning new addresses
- Addresses info important for coding a device driver for the PCI devices
- The PCI bus simplifies the addition and deletion (attachment and detachment) of the system peripherals
- Most used bus in the computer system for interfacing PC-based devices

PCI versions

1. 32/33 MHz,
2. 64/66 MHz,
3. PCI-X 64/100 MHz. version 2.1 has synchronous/asynchronous throughput 132/ 528 MBps [33M×4/ 66M×8 Byte/s]

- Operates on 3.3V to 5V signals
- 1MBps = 1 Mega Bytes per second

PCI versions

4. Super speed version– PCI Super V2.3 264/528 MBps 3.3V (on a 64-bit bus), 132/264 (on a 32-bit bus)
5. Super speed version– PCI-X Super V1.01a for 800MBps 64-bit bus 3.3Volt

PCI signals

100 PCI Bus-Signals

1. Thirty-two lower input/output address lines (like a DMAC, which has both input/output addresses) [Input/output line means to and from a line]
2. Thirty-two higher bits input/output address-cum-data lines (like a DMAC, which has both input/output data and addresses)
3. Clock input to the PCI card/ adapter
4. Reset input to reset the bus as at the start up

100 PCI Bus-Signals

5. Two arbitration input/output lines. A pair of active low bus request- active low bus grant) for PCI use as master (Section 11.14).
6. Parity input/output line
7. Parity 64 output line
8. Two error status and five testing support input/output lines

100 PCI Bus-Signals

9. Ten basic interface input/output protocol lines
10. Four interrupt request output lines
11. One lock control input/output line
12. Two cache support lines

PCI protocol

FIFO controller

- Each device may use a FIFO controller with a FIFO buffer for maximum throughput

Manufacturer assigned ID Numbers

- A manufacturer generally assigned a registered number for global use
- 68HC11 or 80386 are globally registered numbers

ID Numbers

- A 16-bit register in a PCI device identifies this number to let that device auto-detect it
- Another 16-bit register identifies a device ID number
- These two numbers allow the device to carry out its auto-detection by its host computer

Three identification numbers for a device identification of its address space

- (i) I/O port
- (ii) Memory locations
- (iii) Configuration registers of total 256B with a 4-byte unique ID
- These IDs —*VID*: Vendor ID, *DID*: Device ID and *RID*: Revision ID

Address Space Allocation

- Each PCI device has address space allocation of 256 bytes to access it by the host computer
- The unique feature of PCI bus is its configuration address space

Interrupts

- A uniquely assigned interrupt type (a number), which is used for handling the interrupts
- A configuration register number 60 stores the one byte for the interrupt type that defines this unique number

Configuration and common Registers

- 64 bytes for the standard device-independent configuration registers in a PCI device
- Common Register (CR)

Status-register (SR) and Header type (HT) register

- Status-register (SR) and Header type (HT) registers— the compulsorily configured registers
- CBCISB points to card base address
- A PCI controller must access one device at a time

Sharing resources

- All the devices within the host computer can share I/O port addresses and memory locations but cannot share the configuration registers
- A device cannot modify other configuration registers but can access other device resources or share the work or assist the other device

Summary

We learnt

- PCI provides a synchronous parallel communication interface bus
- PCI has 32-bit data bus extendable to 64 bits, 32-bit addresses extendable to 64 bits and total 100 PCI Bus-signals
- Each PCI device address space allocation of 256 bytes to access it by the host computer
- The unique configuration address space in PCI bus

End of Lesson 15 on

Standard I/O bus– PCI