Chapter 11: Input/Output Organisation

Lesson 12:

Bus Arbitration

Objective

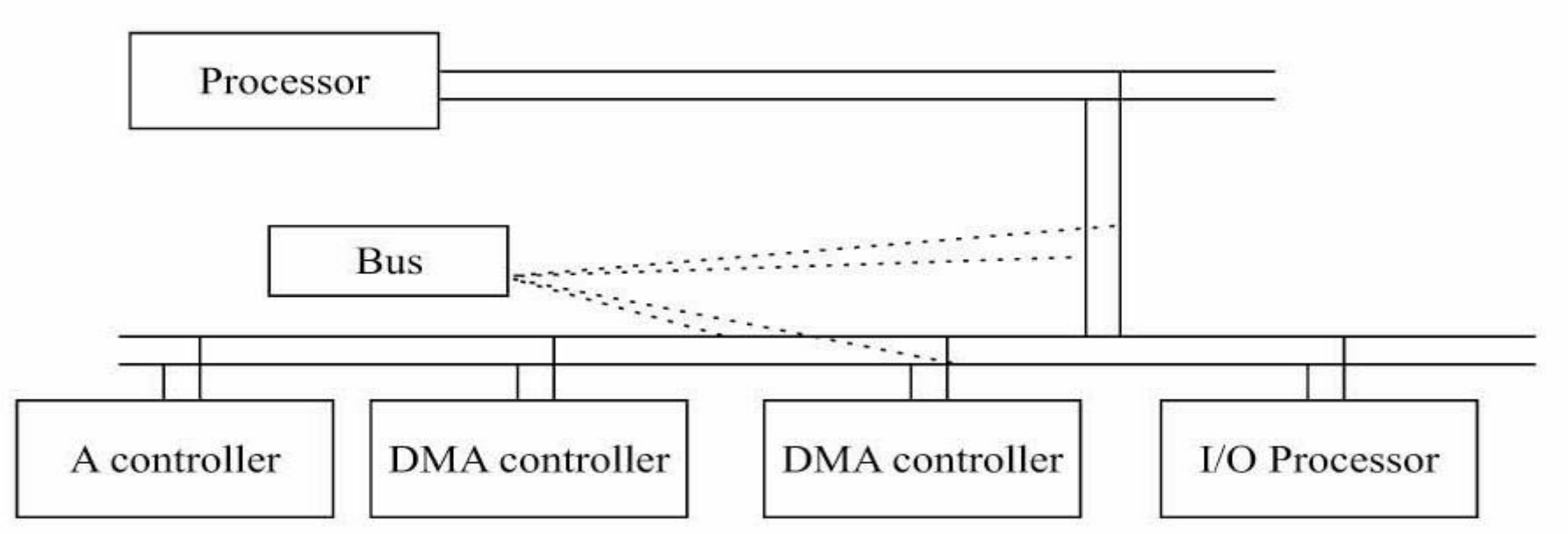
- Be familiar with bus arbitration hardware, daisy chaining, and polling methods of a bus controller

One processor or controller functioning as bus master

A number of DMA or other controllers or processors

- Trying to get access to a bus at the same time, but access can be given to only one of these
- System buses shared between the controller and processor

A number of DMA or other controllers or processors



Only one processor or controller functioning as bus master

- Only one processor or controller can be **bus master**
- The bus master— the controller that has access to a bus at an instance
- Any one controller or processor can be the bus master at the given instance (s)

Bus arbitration process

- *R*efers to a process by which the current bus master accesses and then leaves the control of the bus and passes it to another bus-requesting processor unit

Three bus arbitration processes

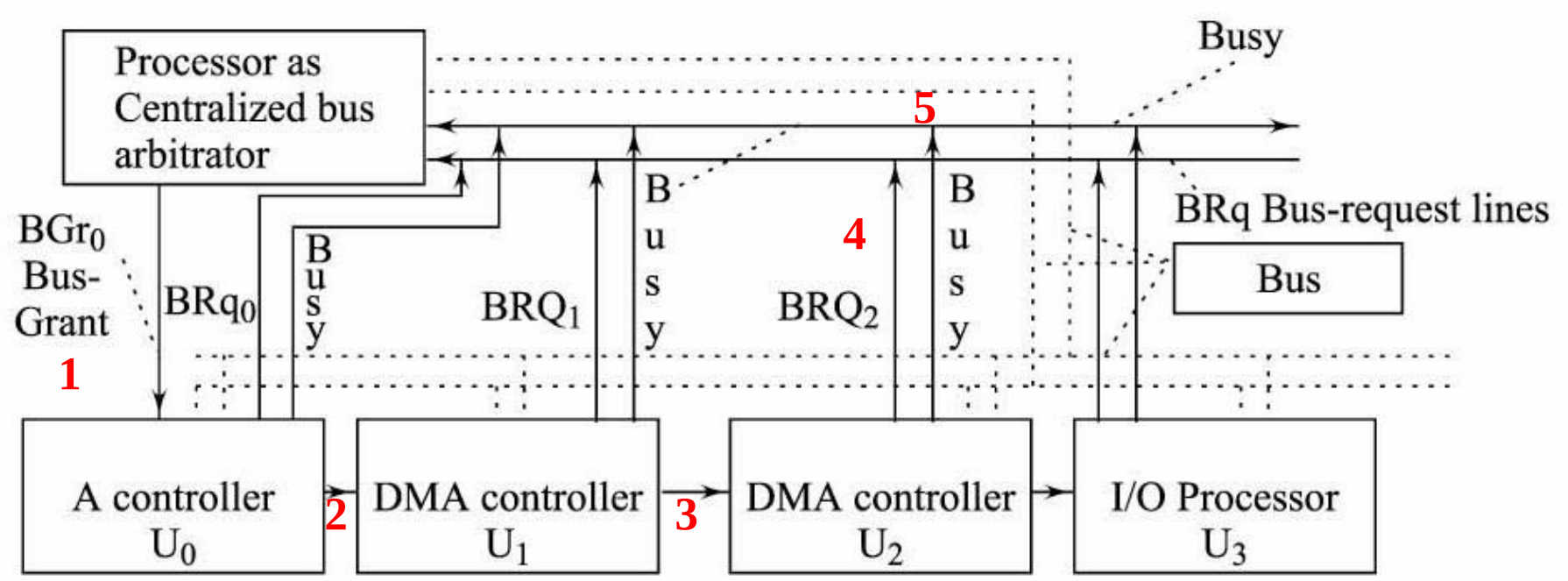
1. Daisy Chain
2. Independent Bus Requests and Grant
3. Polling

Daisy Chaining according to priority

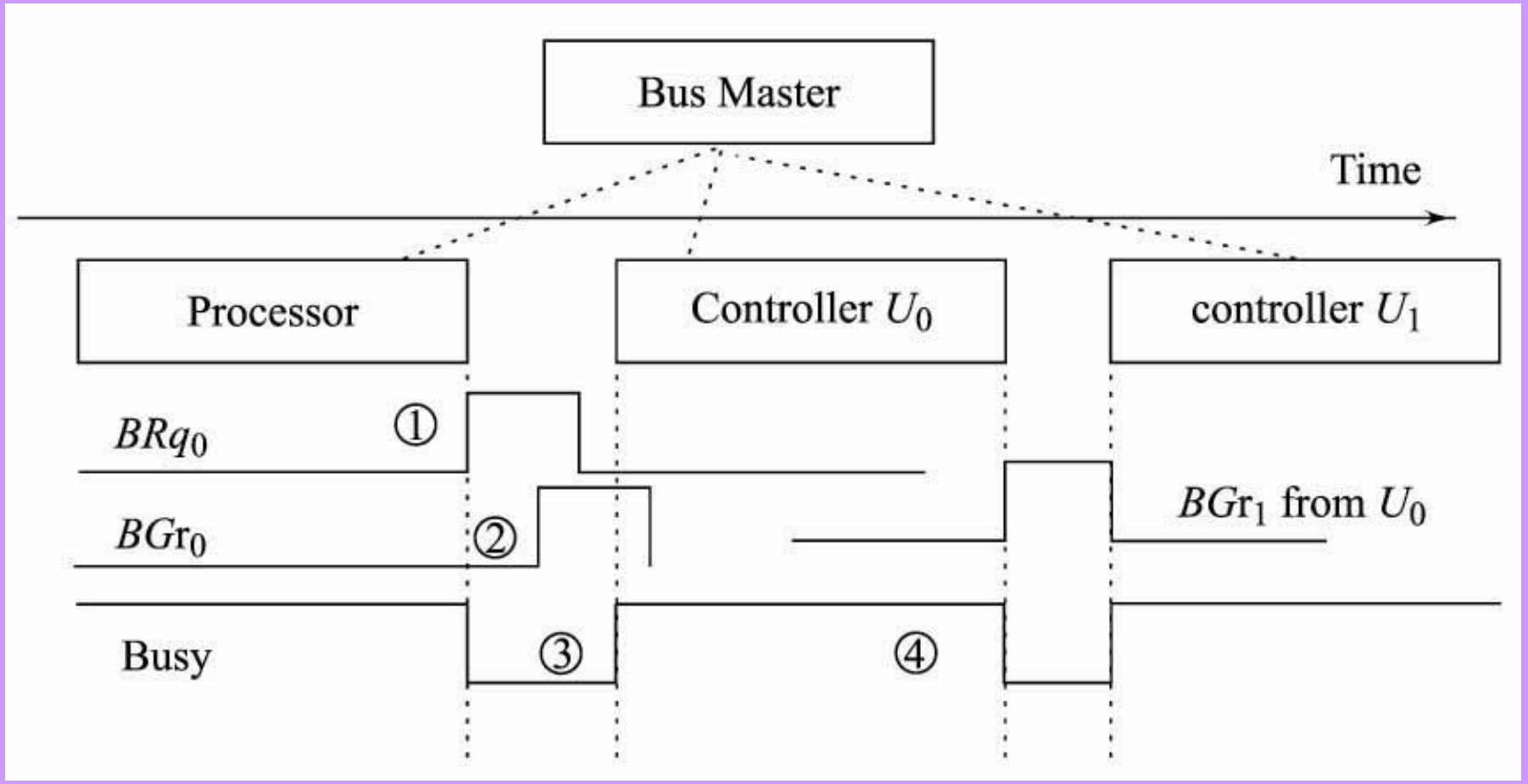
Daisy Chain Method

- A method for a centralized bus arbitration process
- The bus control passes from one bus master to the next one, then to the next and so on
- Bus control passes from unit *U*0 to *U*1, then to *U*2, then *U*3, and so on
- U0 has highest priority, U1 next, and so on

Daisy chaining method



Timing diagram in daisy chaining method method



Step 1

- Bus Grant BGr*i* — This signal means that a unit has been granted bus access and can take control
- Bus grant signal passes from i^{th} unit to $(i+1)^{th}$ unit in daisy chaining when i^{th} unit does not need bus control
- The arbitrator issues only BGr_0

Step 2

- Bus Request BRq*i* — this signal means that *i*-th unit has requested for the grant of the bus access and requests to take control of the bus

Step 3

- Busy─ this signal is to and from a bus master to enables all other units with the bus to note that presently bus access is not possible as one of the units is busy using the bus or has been granted control over the bus
- The unit, which accepts the BGr, issues the *Busy*

Independent Bus-Request and Grant Method

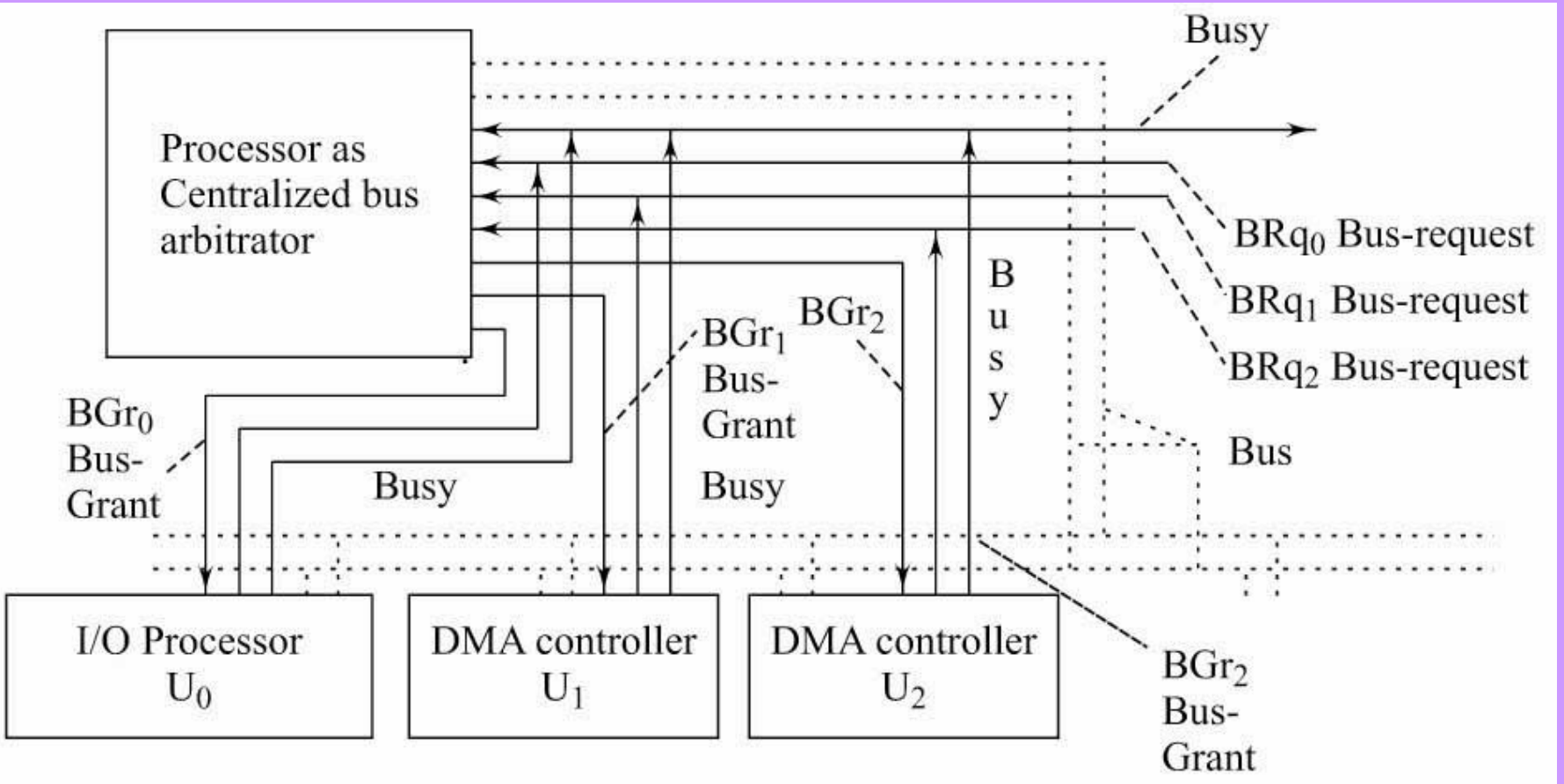
Bus independent requests and grants method

- The bus control passes from one bus master to another only through the centralized bus controller
- Assume *n* units can be granted bus master status by a centralized processor as bus controller after listening to its request

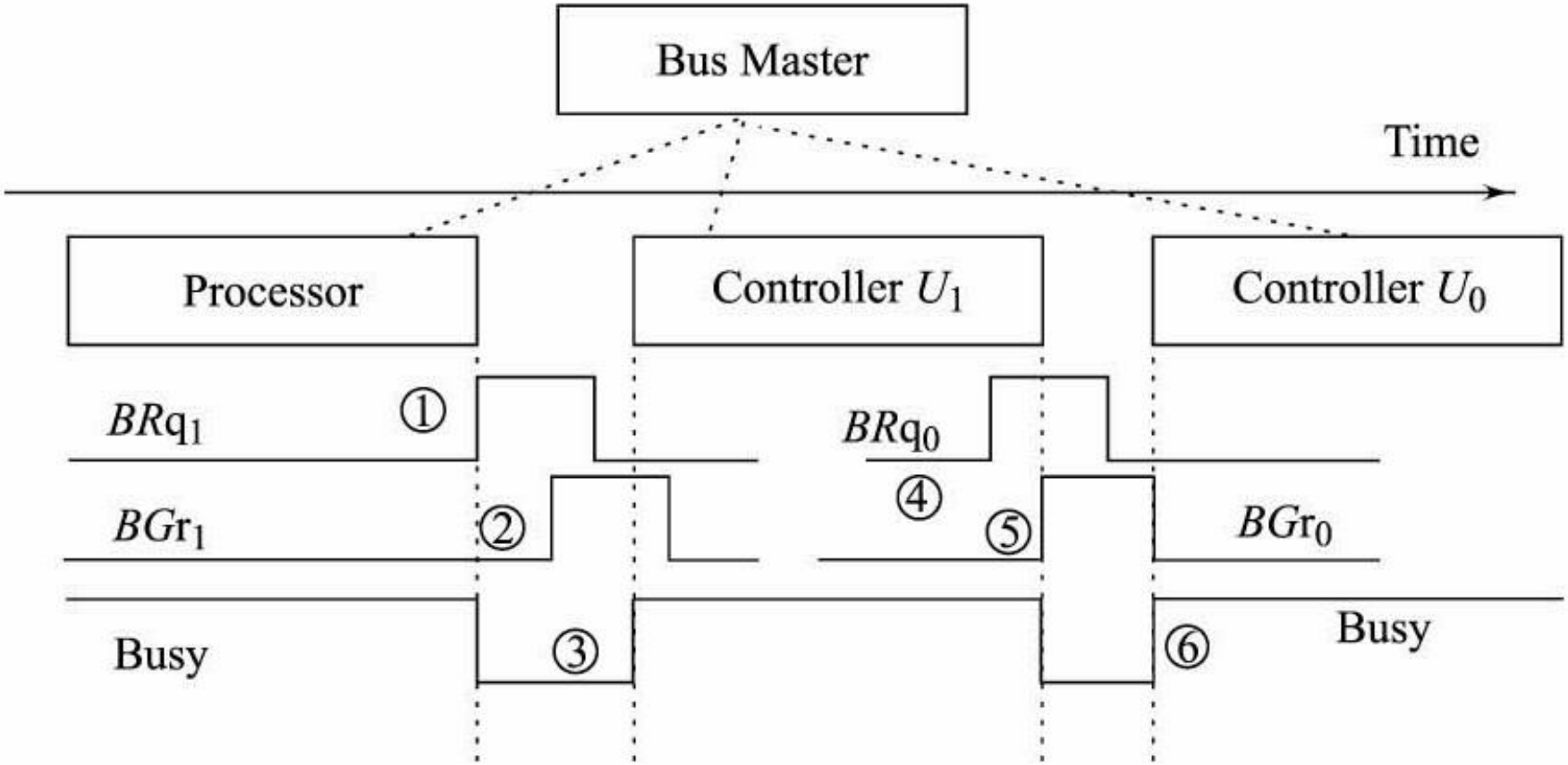
Independent request method

- The centralized controller listens to requests of each device individually and grant access to the bus
- If number of requests pending, then grant by a priority resolution algorithm which resolves the priority issue

Bus control passing from a bus master to another only grant of bus on an independent request



Timing diagram in independent bus request and grant method



Step 1

- Bus Request BRq_i for $i = 0$ to $n - 1$
- BRq_i— this signal means that i^{th} unit has requested for the grant of the bus access and requests to take control of the bus

Step 2

- Bus Grant BGr_i for $i = 0$ to $n - 1$
- BGr_i signal means that i^{th} unit has been granted bus access and can take control
- Bus grant signal passes to any i^{th} unit from the centralized processor only after the unit sends i th BRq_i

Step 3

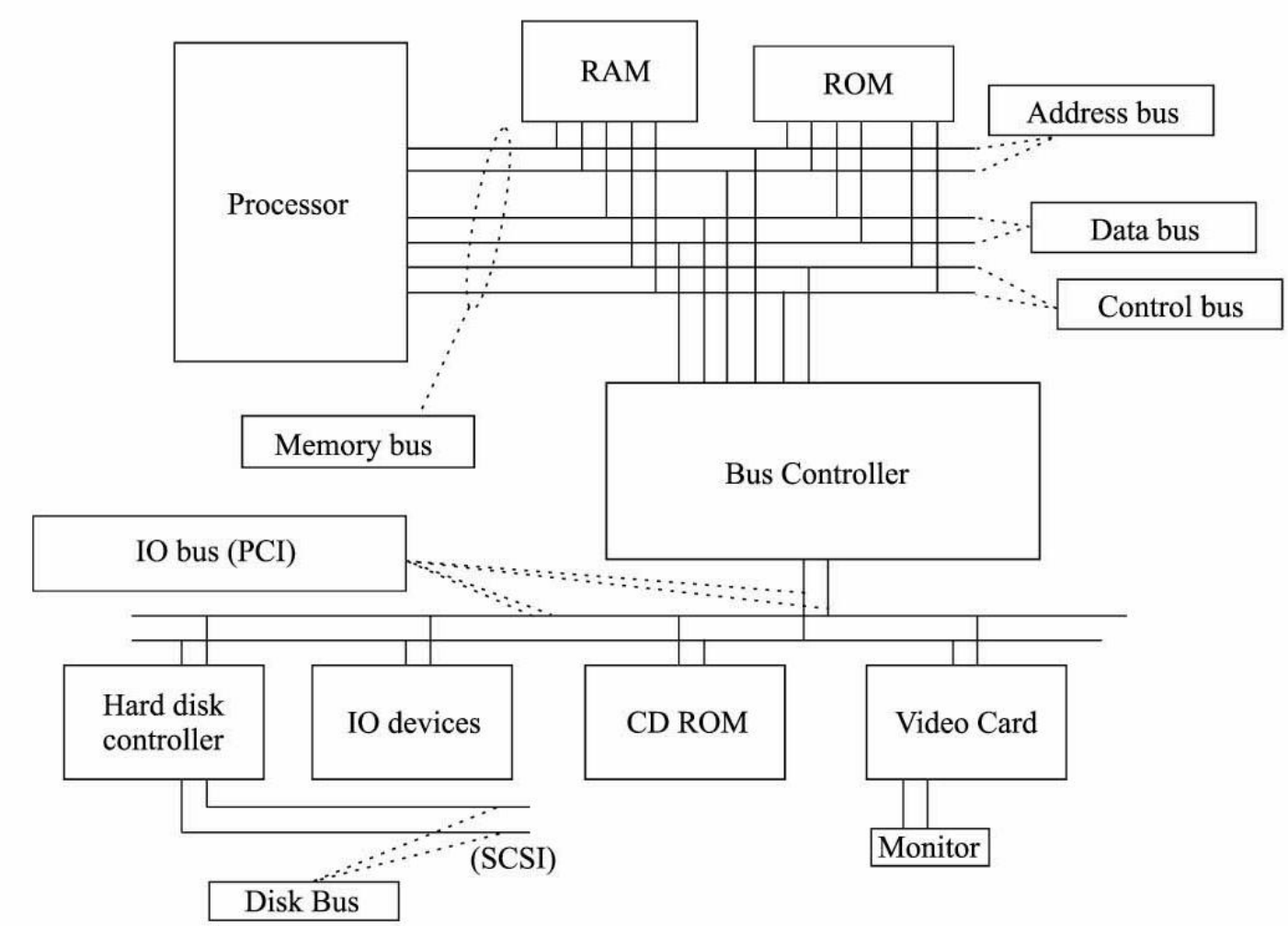
- Busy— this signal is from a bus master to enable all other units with the bus to note that presently bus access is not possible as one of the units is busy using the bus or has been granted control over the bus

Polling Method

Bus polling method

- The bus control passes from one processor (bus controller) to another only through the centralized bus controller, but only when the controller sends poll count bits, which correspond to the unit number
- Assume *n* units can be granted bus master status by a centralized processor

Bus polling method



Step 1

- Bus Poll Count BPC (on three lines for a *Ui* where $i = 0$ to $n - 1$ or $n = 8$)
- The count = c means that $(2^c - 1)$th unit being polled for the grant of bus access and can take control from the processor
- Bus count lines connect to each unit from the centralized processor

Step 2

- Bus Request BRq_i for $i = 0$ to $n - 1$
- This signal means that the i^{th} unit has accepted the grant of the bus available access and requests to take control of the bus

Step 3

- Busy— this signal is from a bus master to enable all other units with the bus to note that presently bus access is not possible as one of the units is busy in using the bus or has been granted control over the bus

Summary

We learnt

- Bus arbitration hardware three methods, daisy chaining, and polling methods of a bus controller
- Daisy chaining, the centralized controller always sending bus control to highest priority, which passes it to next if bus access not required
- Independent request method, the centralized controller listens to requests of each device individually and grant access to the bus on resolving its priority

We learnt

- Polling methods method, the centralized controller does the polling of the devices and grant access to that bus which requests it on receiving the poll count

End of Lesson 12 on

Bus Arbitration