Chapter 11: Input/Output Organisation

Lesson 11:

Input-Output Processor

Objective

- Understand processing at an IOP (Input-Output Processor)
- Learn about parameters in a multi-channel IOP at the memory block for IOP
- Learn about 8059 a four channel IOP

I/O Processor

IOP (I/O processor)

- A specialized processor
- Not only loads and stores into memory but also can execute instructions, which are among a set of I/O instructions
- The IOP interfaces to the system and devices
- The sequence of events involved in I/O transfers to move or operate the results of an I/O operation into the main memory (using a program for IOP, which is also in main memory)

IOP

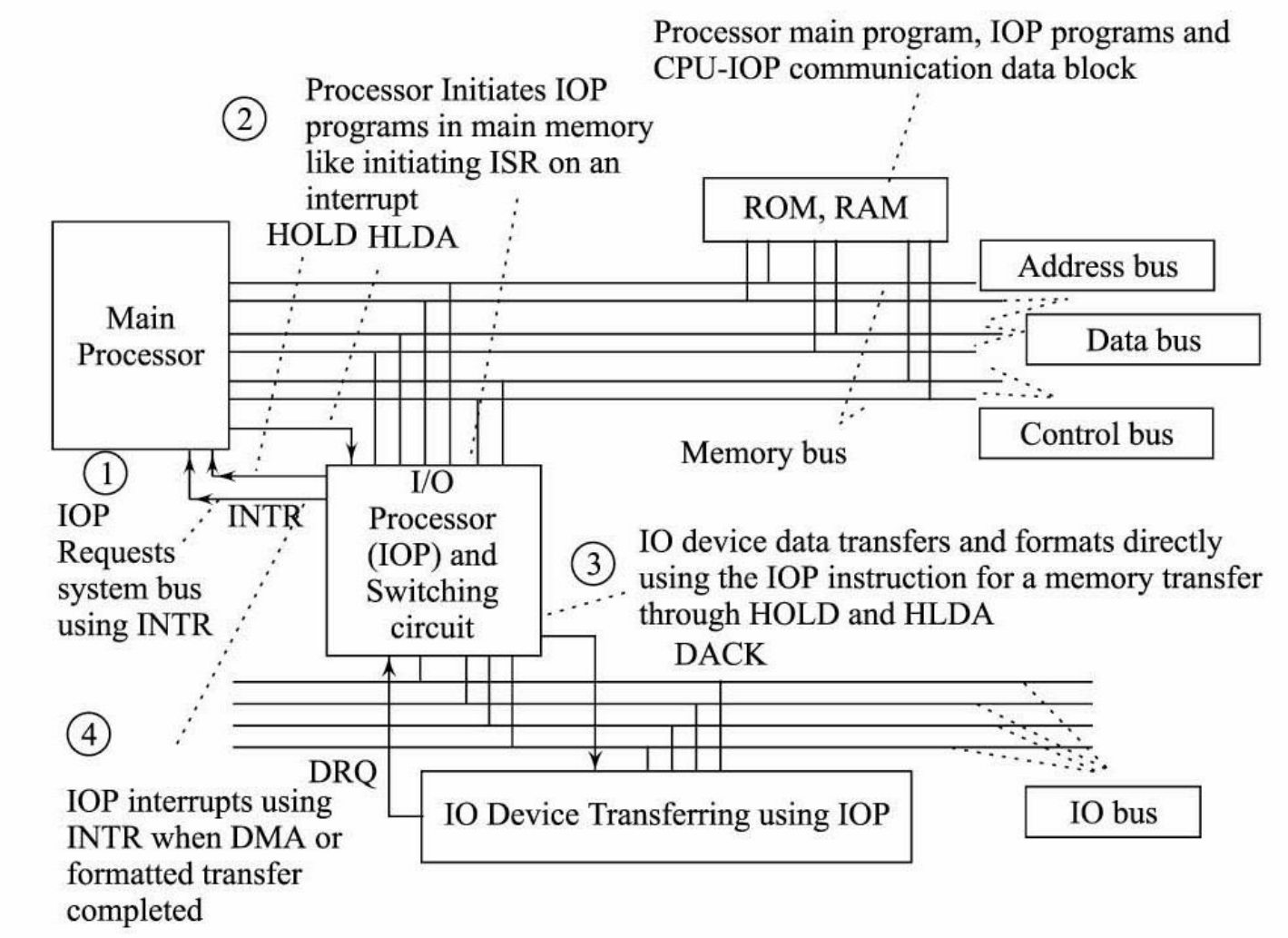
- Used to address the problem of direct transfer after executing the necessary format conversion or other instructions
- In an IOP-based system, I/O devices can directly access the memory without intervention by the processor

IOP instructions

- Instructions help in format conversions─ byte from memory as packed decimals to the output device for line-printer
- The I/O device data in different format can be transferred to main memory using an IOP

Sequence of events when using an I/O Processor

Sequence of events involved in I/O transfers



Sequence 1 ad 2 of events

- Sequence 1: A DRQ (for IOP request) signal from an IOP device starts the IOP sequence, the IOP signals an interrupt on INTR line this requests attention from the processor
- Sequence 2: The processor responds by checking the device's status via the memory-mapped control registers and issues a command telling the IOP to execute IOP instructions for the transfer to move the formatted data into the memory.

Sequence 3 of events

- *Sequence 3:* During each successive formatted byte(s) transfer, the device DMAC (DMA controller) logic inside the IOP uses a processor bushold request line, HOLD, distinct from INTR device interrupt request line
- The main processor sends to the device a signal from the processor called DACK (distinct from INTA device-interrupt request-acknowledge line)

Sequence 3 of events

- The I/O device bus has access to the address and data buses of the memory bus when DACK is activated
- It has no access when DACK is not activated when a HOLD request is not accepted by the processor when the processor is using the memory bus

Sequence 3 of events

- Once the DMA logic start command has been issued to IOP, the main processor begins working on something else while the I/O device transfers the data into the memory

Sequence 4 of events

- Sequence 4: When the IOP's DMA transfer as per instructions is complete, the I/O device signals another interrupt (using DRQ)
- Lets the main processor know that the DMA is done and it may access the data

8059 an exemplary four-channel IOP

8059

- Simple data type operations and has simple addressing modes
- Instructions are for setting interrupt, bus width format setting during transfers, arithmetic operations like increment, decrement, and add unsigned and signed fixed point numbers

8059

- IOP and CPU programs are both in memory
- A common region for CPU and IOP through which two programs can access a common data block

8059

- Instead of DMAC registers, this block in memory is used by the IOP
- The CPU program uses this block to load the value of the control parameters for the IOPs for each channel

Parameters in a multichannel IOP at the memory block for IOP

Typical parameters in a multichannel IOP at the memory block for IOP

- At the block, at the start address, a set of words each for a channel

(i) pointer for the channel parameter block start address

(ii) status for each channel

(iii) the channel command (action to be done— for example input (load) or output (store) operation

Typical parameters in a multichannel IOP at the memory block for IOP

- A pointer to the channel IOP program at each channel parameter block start address
- After that parameters corresponding to that program

IOP channel parameters for the IOP DMA logic

Channel parameters for the IOP DMA logic

1. PC_i (Program Counter) for i^{th} channel IOP instruction for sending the memory address during memory access),
2. $IOAR_i$ (i^{th} channel I/O Device register/buffer Address Register for IOP sending the I/O address during an I/O access)

Channel parameters for the IOP DMA logic

3. DC_i (Data Count) register for *i* th channel to enable counting of the transfer of bytes after IOP operation as the DC, later on, decrementing in sequence 3 on successive transfers, enables interrupt of processor on terminal count at sequence 4

IOP parameters

4. (i) Program a bit to issue a terminal count interrupt after every N bytes transfer during sequence 2 as well as at the end of the terminal count in DC

(ii) To program the channel number and resolve channel priorities in case multiple I/O channel programs are used

Summary

We learnt

- Processing of instructions also in addition to DMA logic at an IOP (Input-Output Processor)
- Parameters in a multichannel IOP at the memory block for IOP
- 8059 a four channel IOP

End of Lesson 11 on

Input-Output Processor