Chapter 11: Input/Output Organisation

Lesson 02:

Accessing the I/O devices and Interface circuit

Objective

- Understand how a processor accesses and addresses the I/O peripheral devices
- Understand the addressing of the multiple devices to get access to a bus for the IO

IO Interfacing Features for accessing I/O devices

IO Interface functions

- A computer provides for IO interfaces for accessing the I/O devices
- Interface connects an IO peripheral device to the computer system buses
- Enables communication of input from the device to computer and output from the computer to device

Features of IO subsystem

(i) Slow operations compared to processor-memory operations

(ii) Slow rate of data transfer to and from processor

Features of IO subsystem

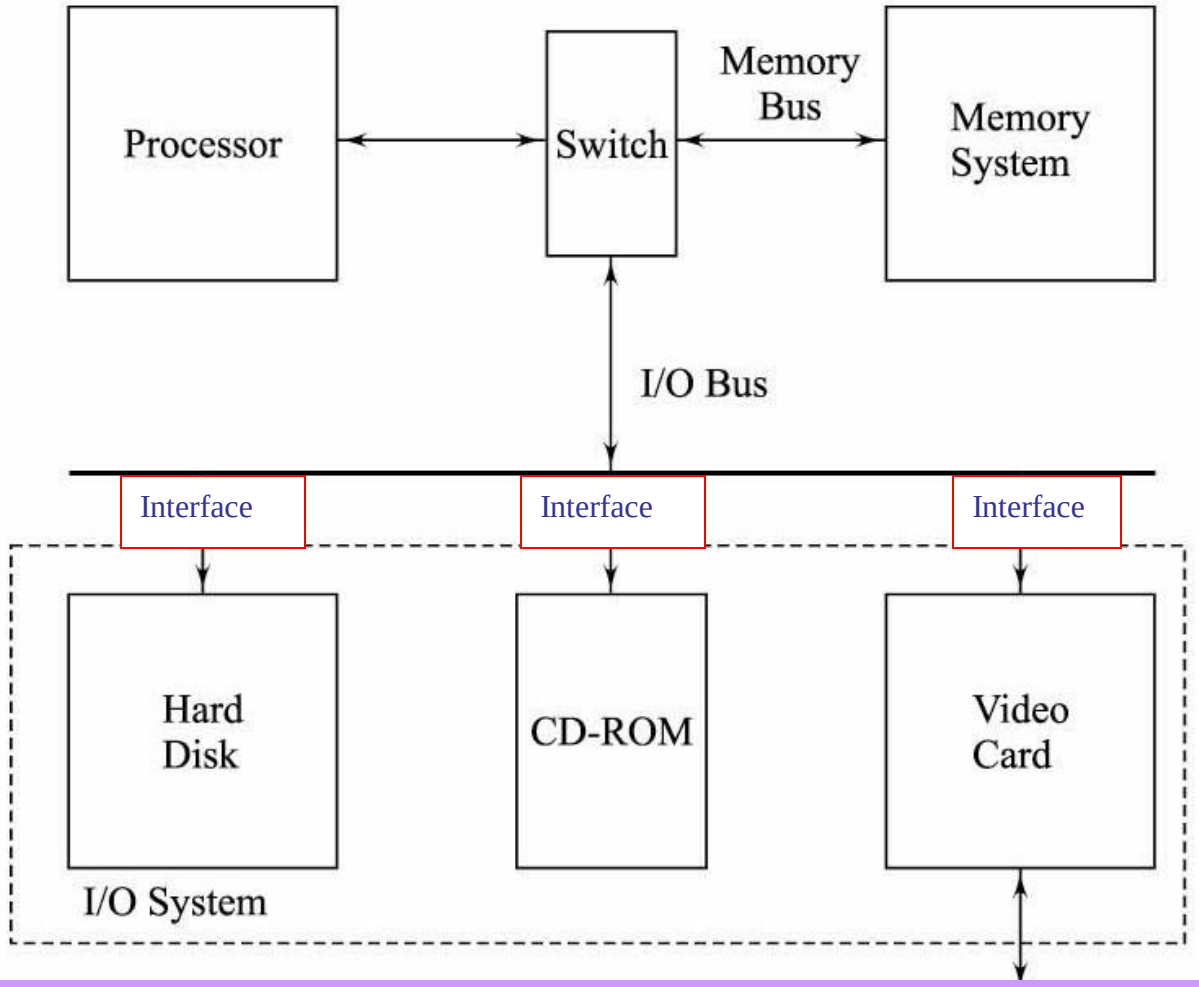
(iii) Different format of data transfer

- While format is 32-bit word for data transfer between memory and processor, the format may be ASCII characters for the touch screen or printer and may be just one bit to a valve in washing machine or input from a switch or phototransistor

Features of IO subsystem

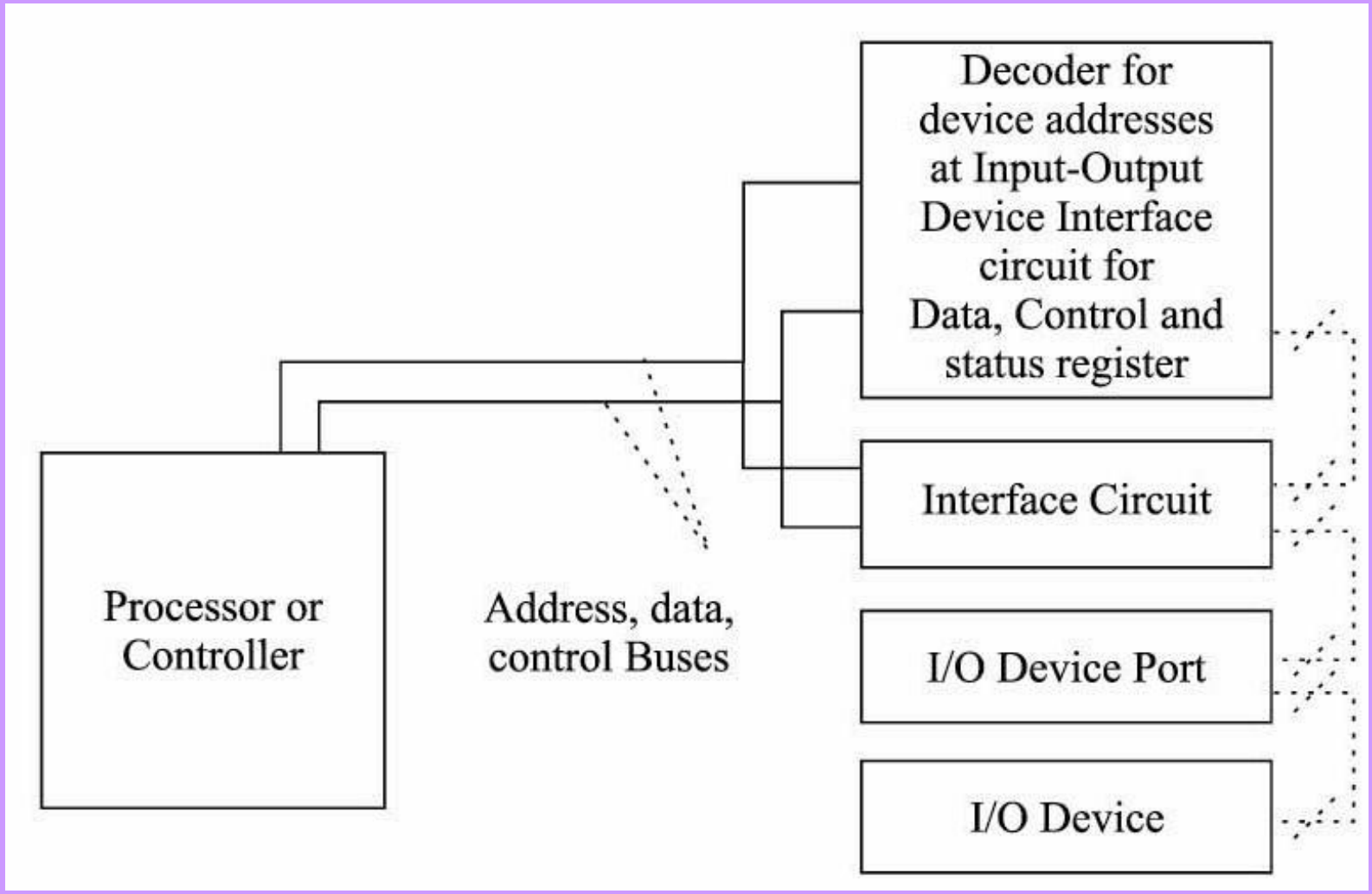
(iv) Different mode of functioning in the device and computer

Simple view of processor, memory bus, IO bus and interconnection (interface) to IO devices



Processor access and interface to I/O device

IO device Interfacing the bus using address decoder and IO interface circuit



Processor access and interface to I/O device

(i) Control (command) register(s): This acts as a command register and is used to tell the device what the processor wants it to do

Processor access and interface to I/O device

(ii) Status register(s): This is used to tell the processor what the present status of the device is; for example whether ready, whether it has finished the previously commanded action, whether the input buffer has data still to be read by the processor, or whether the output buffer for sending the output of the device is empty

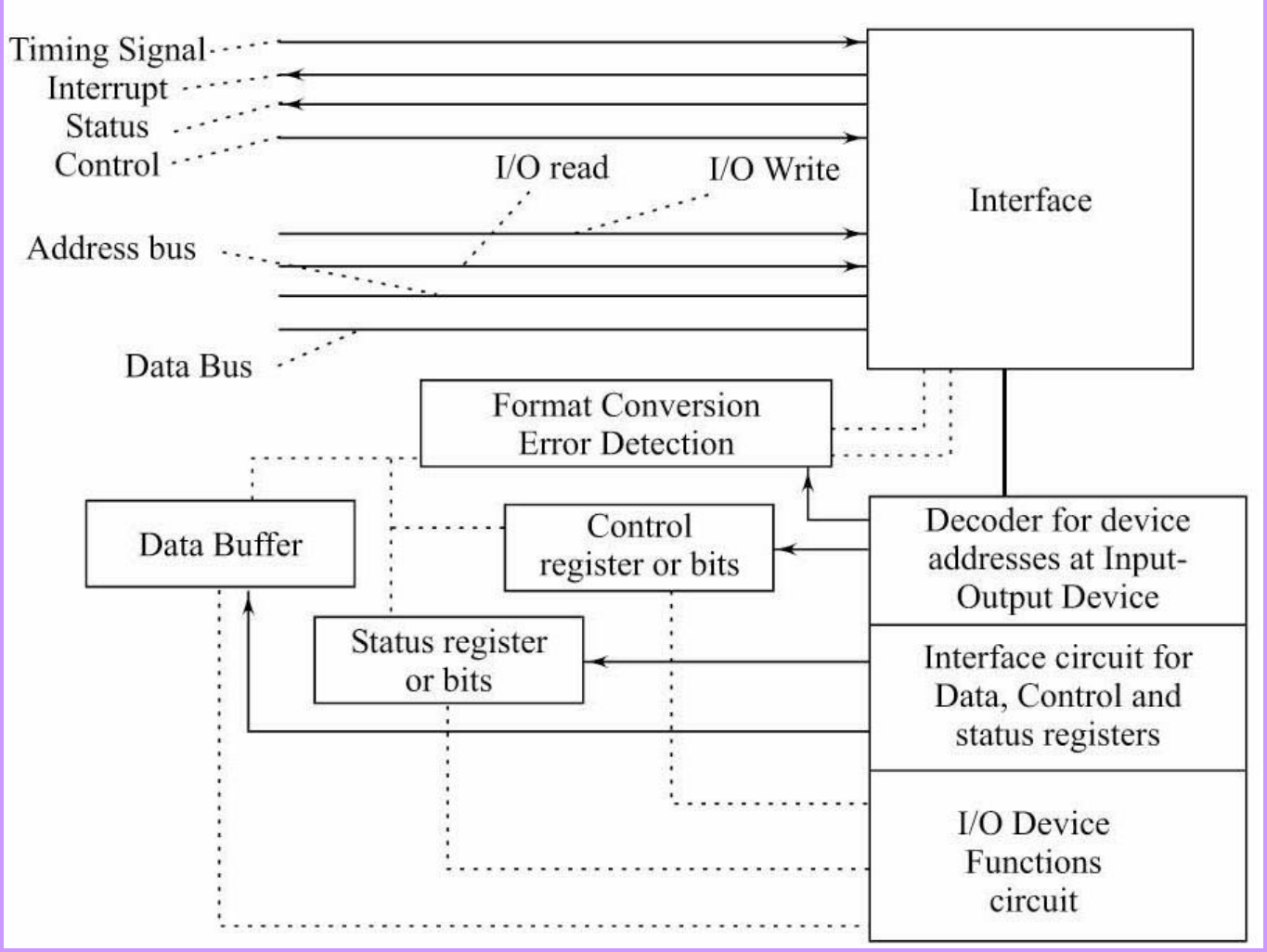
Processor access and interface to I/O device

(iii) Output register(s) or buffer, for sending the output through the device

Processor access and interface to I/O device

(iv) Input register(s) or buffer for receiving the input from the device

Interface circuit in-between the bus and IO device

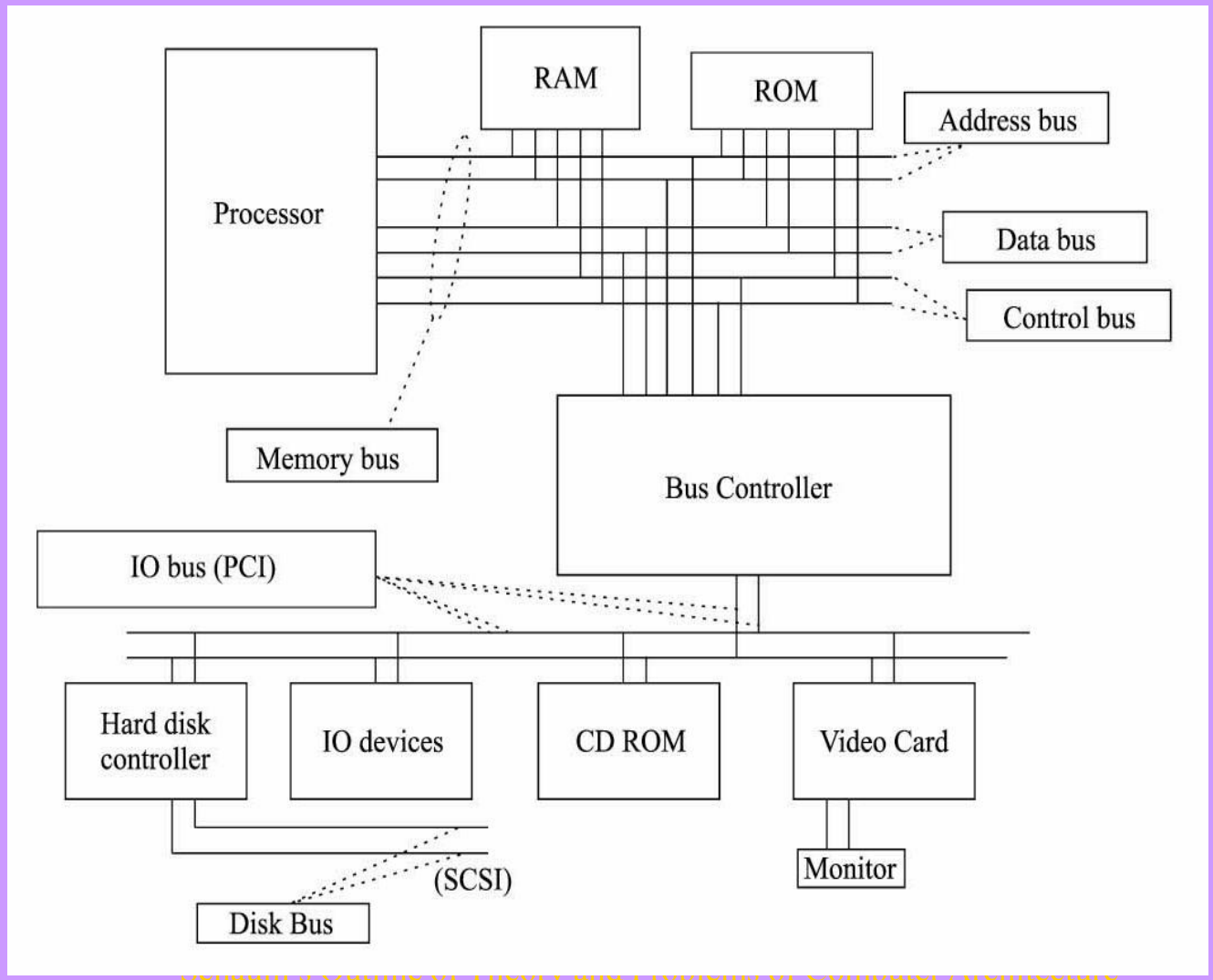


Separate Memory and I/O Buses used to Communicate with the Memory System

Separate Memory and I/O Buses used to Communicate with the Memory System

- I/O System using the Bus Controller and Separate Disk I/O Bus

Separate Memory and I/O Buses used to Communicate with the Memory System



The I/O bus

- Creates an interface abstraction that follows the processor to interface with a wide range of I/O devices using a very limited set of interface hardware

Addition of devices with a system's IO bus

- A device that is compatible with a particular I/O bus can be integrated into any system that uses that type of bus

Addition of devices with a system's IO bus

- Systems that use I/O buses, as opposed to direct connections between the processor and each I/O device, very flexible, allowing a system to support many different I/O devices depending on the needs of its users and allowing users to change the I/O devices that are attached to a system as their needs change

Timings for Assessing the I/O Bus

Example

- Assume— a bus requires 5 ns for requests, 5 ns for arbitration, and takes an average of 7.5 ns to complete an operation once access to the bus is granted
- Find whether the bus perform can 50 million operations per second

Solution

- To achieve 50 million operations/s, each operation must complete in an average of 20 ns
- Adding the request, arbitration, and average completion times for this bus gives an average time of 17.5 ns per operation
- Thus, the bus will be able to complete more than 50 million operations per second on average time

Timings for Assessing the I/O Bus

- The time to perform an operation on a bus is the sum of the time for a device to request use of the bus, the time to perform arbitration (decide which device can use the bus), and the time to complete the operation once a device has been granted access to the bus

Bus protocol limiting Timings for Assessing the I/O Bus

Bus protocols

- Some bus protocols may place limits on the amount of time that a single operation can take to complete, to ensure that high-priority devices cannot be prevented from using the bus by long-latency operations initiated by low-priority devices

Summary

We Learnt

- Accessing the IO devices
- Slow operations
- Slow data transfer
- Different formats of data transfer
- Different modes
- Separate IO bus

We Learnt

- The time to perform an operation on a bus is the sum of the time for a device to request use of the bus, the time to perform arbitration (decide which device can use the bus), and the time to complete the operation once a device has been granted access to the bus
- Bus protocol timings for the operations

End of Lesson 02 on

Accessing the I/O devices and Interface circuit