Chapter 08: The Memory System

Lesson 08:

Synchronous DRAM (SDRAM) and DDR-SDRAM

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Objective

- Understand DRAMs in which clock input synchronises the RAS-CAS cycles and there exists the pipelined Access

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Synchronous DRAM (SDRAM)

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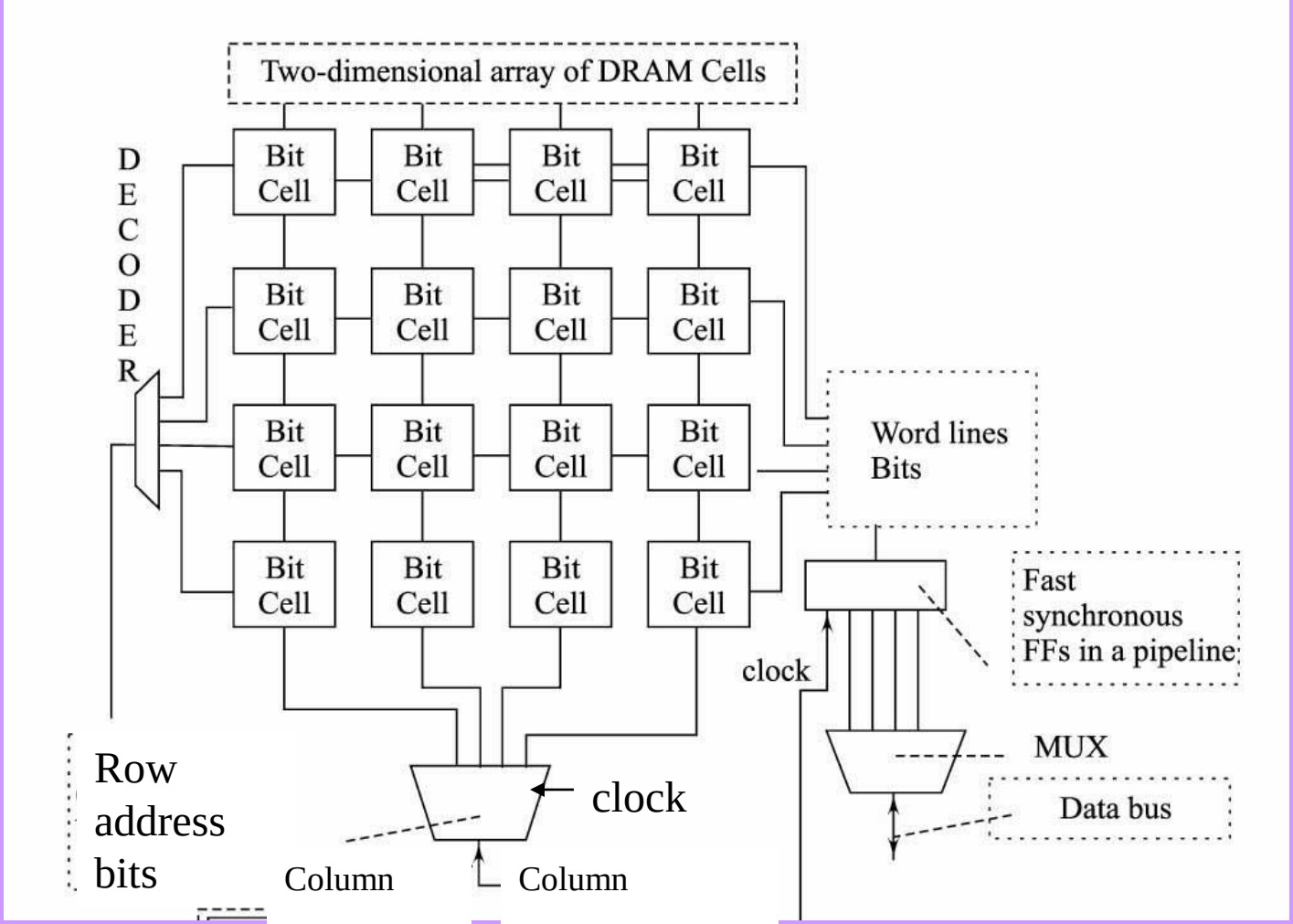
Access in SDRAM using clocked latch and clocked sequencer



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SDRAM Sequencer

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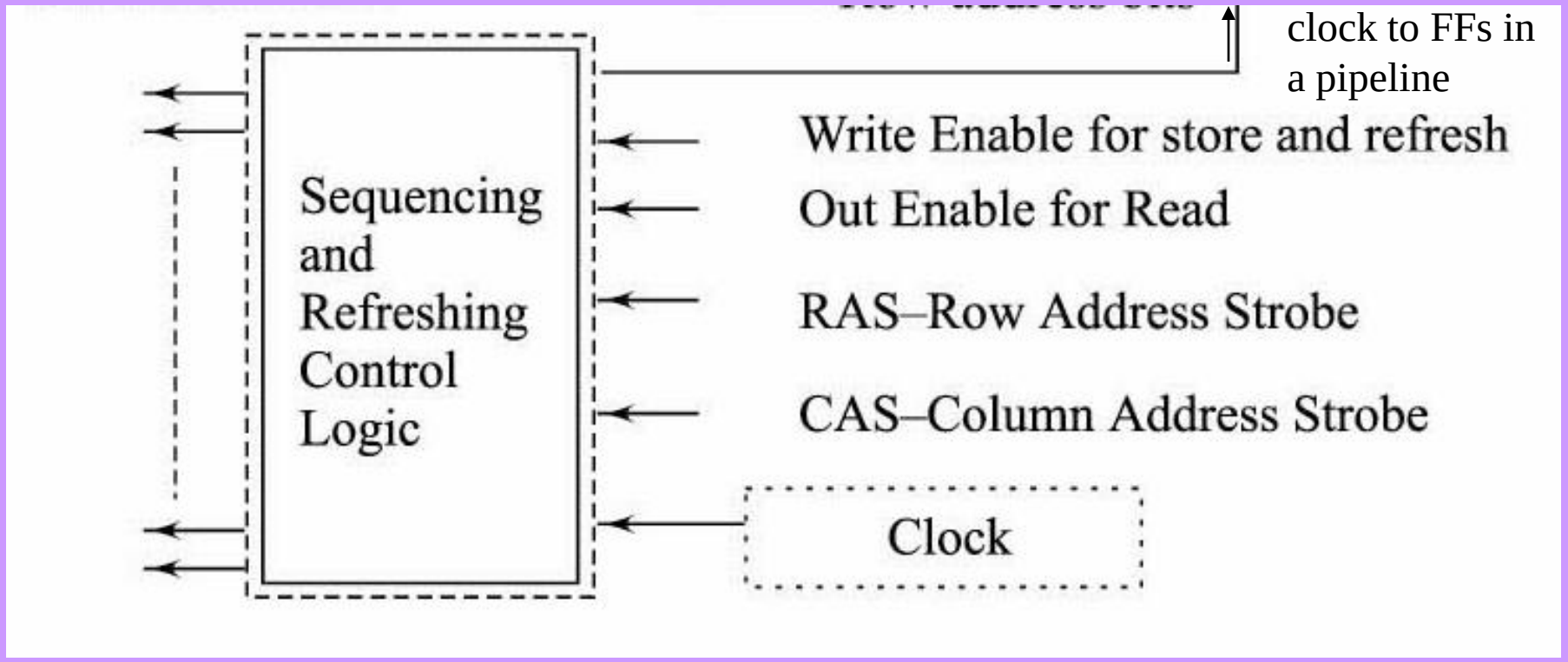
Sequencer in SDRAM



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SDRAM Features

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Synchronous DRAMs (SDRAMs)

- These devices similar to fast page-mode DRAMs
- SDRAM requires an additional clock input (other DRAMs are asynchronous devices)
- On each clock input the row changes to next ones till n rows
- n-rows are pipelined and accessed

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DDR-SDRAMs

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DDR SDRAMS

- The SDRAMs increase throughput by pipelining and interleaving
- Most SDRAMs are pipelined, and many provide access modes, for example, double data rate SDRAM (DDR SDRAM), by two-way address interleaving, that allow multiple sequential words of data to be written with just one RAS-CAS cycle, further increasing bandwidth.

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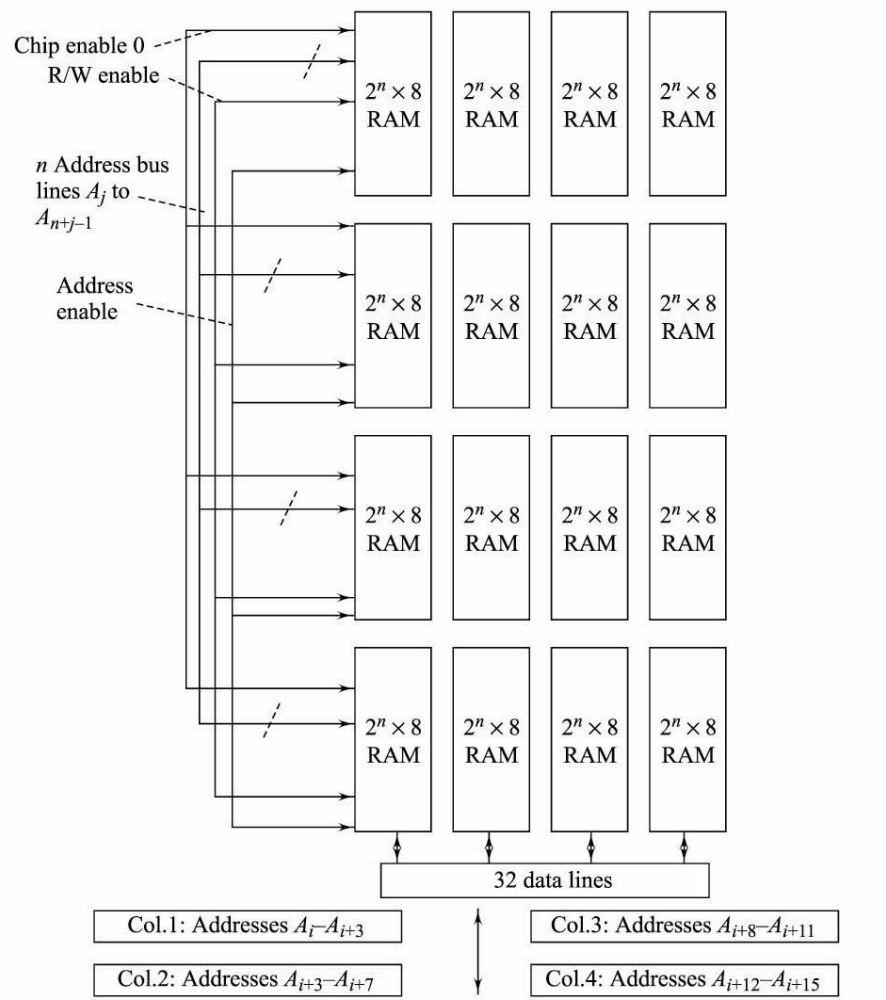
DDR synchronous DRAM organisation by two interleaved SDRAMs



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RDRAMs (RAMbus DRAMs)

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RDRAM

- A proprietary bus called Rambus
- RDRAM– DRAMs consisting of multiple columns of cells interfacing the RAMbus

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- RDRAMs share a common RAMbus
- Operate the bus at low voltage
- Operate the less wide than 32-bit allow faster clock rate (400 MHz plus) operations on the bus

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Bus control signals

1. Bus control
2. Bus enable
3. Transmitter clock
4. Receiver clock

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Bus control signals

5. Reference voltage ~ 2V for DRAM
6. 9 bit data bus with logic 1 and 0 as per reference voltage and ~ 0.3V, respectively
7. Power.
8. RDRAM select bits

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RDRAM

- An RDRAM─ a slave of a master controller (a CPU) and communicates at low voltages and low data bus width, enabling fast data accesses to the interleaved SDRAMs

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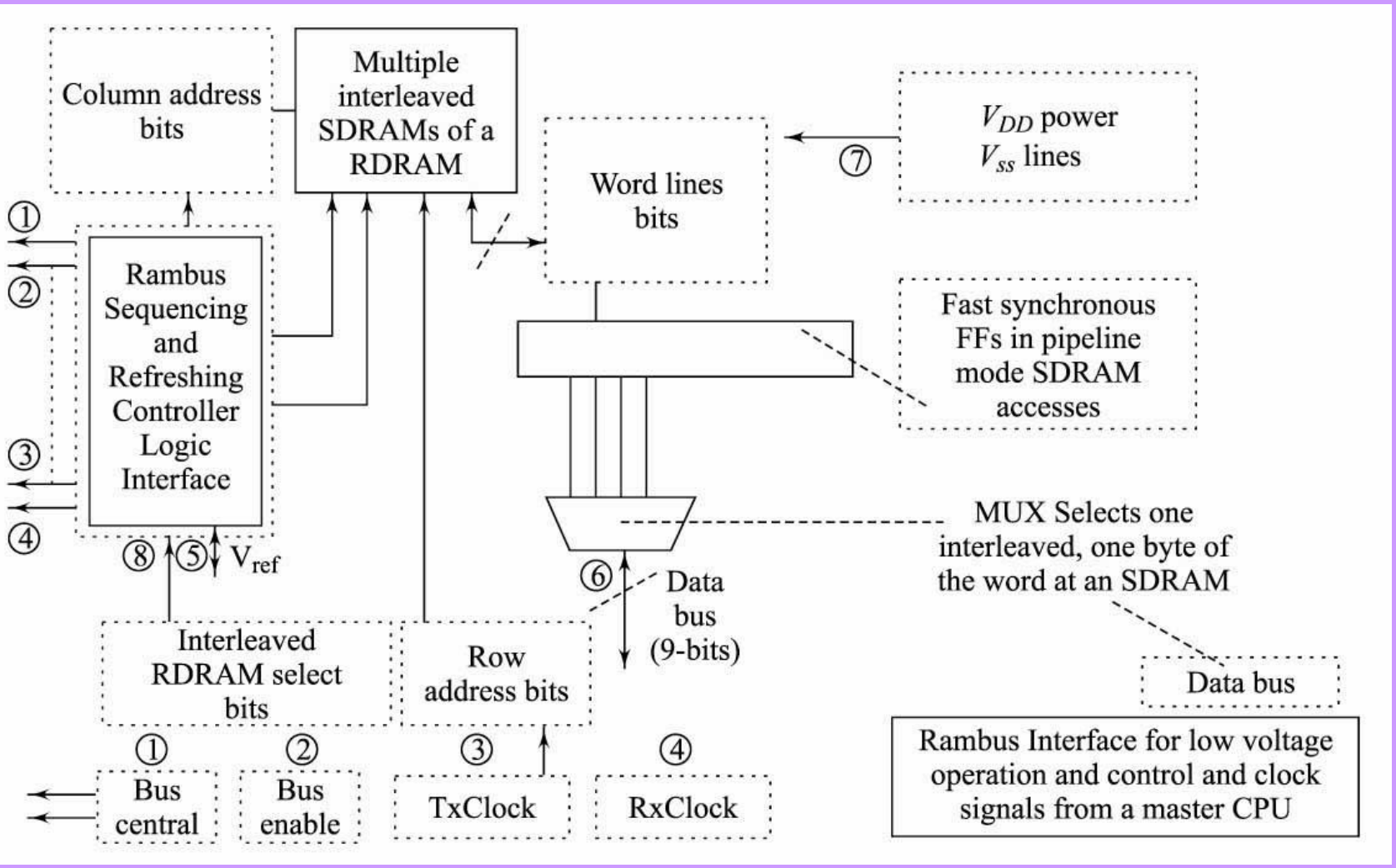
RAMbus DRAM organisatiom



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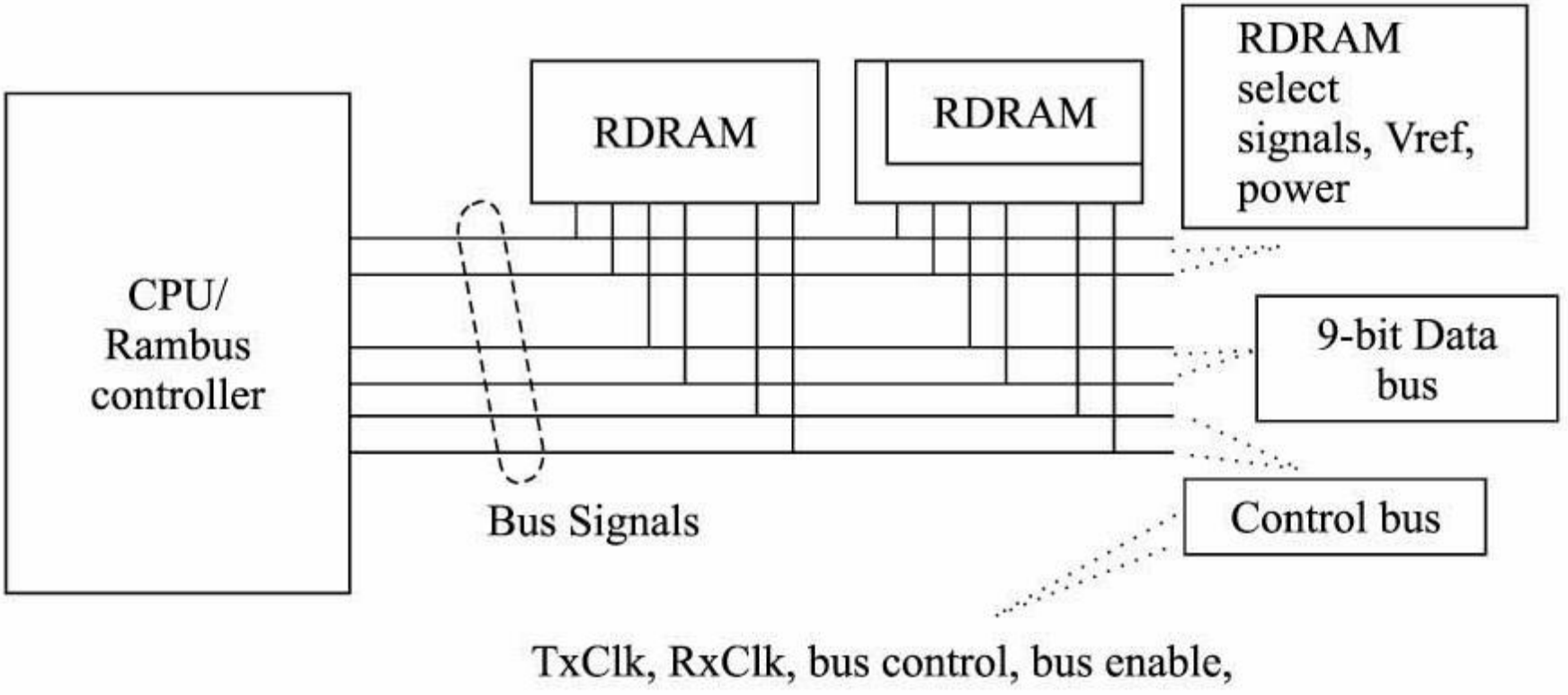

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Summary

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We learnt

- SDRAM uses a clock to synchronous strobe of the column and row addresses and the FFs in the pipelined output
- Pipelined access in SDRAM
- DDR-SDRAMs use the pipelined and Interleaved accesses
- RAMbus based accesses of the RDRAMs
- RAMbus operate at low voltages and less than 32-bit wide bus

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End of Lesson 08 on

Synchronous DRAM (SDRAM) and DDR-SDRAM

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