Chapter 08: The Memory System

Lesson 06:

Asynchronous Dynamic RAMs (DRAMs) and Access cycles and access time in Asynchronous DRAM in normal mode

Objective

- Understand asynchronous access DRAM
- Learn total access time computation in asynchronous DRAM operations in normal mode page modes

Asynchronous DRAM

DRAM REFRESH

- DRAMs function as dynamic RAMs because the values stored in each bit cell are not stable
- Over time, leakage currents will cause the charge stored on the capacitor to drain away and be lost
- To prevent the contents of a DRAM from being lost, the DRAM must be refreshed

Refresh Operation

- Reads the contents of each bit cell in a row of the bit cell array
- Then it writes the same values back into the bit cells
- Restores them to their original value

DRAM Refresh Time

- As long as each row in a DRAM refreshed sufficiently frequently that none of its capacitors' charges decay low enough that the hardware misinterprets the values stored in the row, the DRAM can hold its contents indefinitely

DRAM Chip Specifications

- Refresh time─ how often a row can go without being refreshed before it is in danger of losing its contents

Example 1

- Assume─ DRAM has 512 rows
- Refresh time is 10 ms

Solution for how often (on average) a row refresh operation need to be done

- Refresh time = 10 ms
- Each row needs to be refreshed at least once every 10 ms
- Number of 512 rows
- 512 row refresh operations in each 10-ms period
- An average of 1 row refreshed every 1.95×10^{-5} s

Example 2

- Assume─ DRAM has 1024 rows in its array of bit cells
- Refresh time = 8 ms
- Each row refresh operation takes 100 ns
- Find how often must a row refresh operation be performed on average
- Also, find fraction of the DRAM'S time spent performing refreshes

Solution

- Each row must be refreshed once every refresh time
- 1024 row refresh operations must be done every 8 ms
- 1 row refreshes every = 8 ms /1024 = 7.8 microseconds on average
- Each row refresh takes 100ns, so the fraction of the DRAMS time taken by row refreshes is 100 ns/7.8 microseconds = 1.28 percent

Distribution of Row Refreshes

- A designer decides how those row refreshes are distributed across the 10-ms period
- They can be distributed evenly
- Done as a block of row refreshes at the start of each period, or anything in between

Row and Columns Accesses in Normal mode

- Unlike SRAMs, the address input to a DRAM is divided into two parts
- The row and the column addresses
- Sent to the DRAM in separate operations
- Typically, the high bits of a memory address are used for the row address
- The low bits are used for the column address

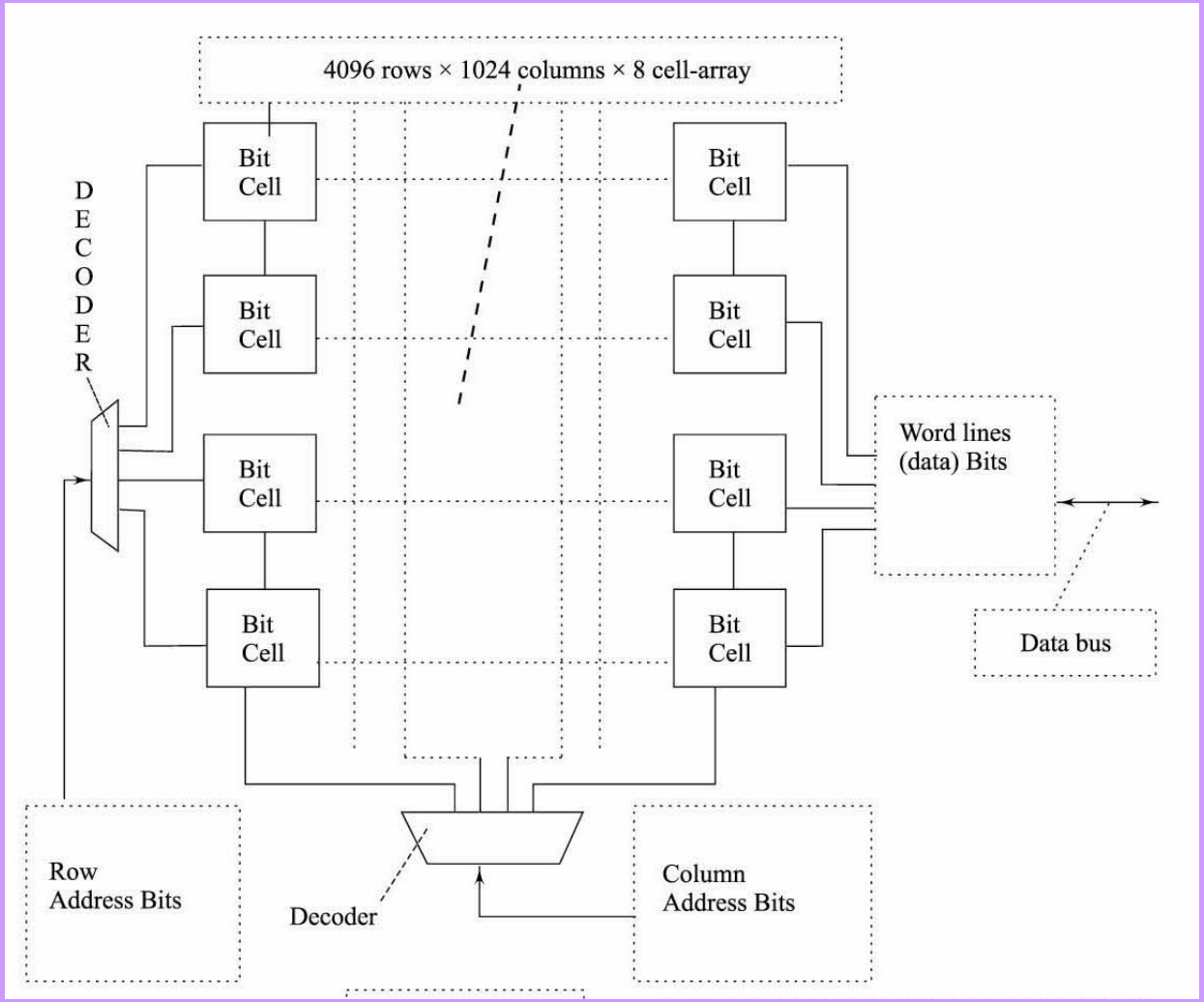
Row Address accesses in Normal mode

- As might be expected from the name, the row address selects the row of the DRAM array that is being referenced, while the column address selects a bit or set of bits out of that row

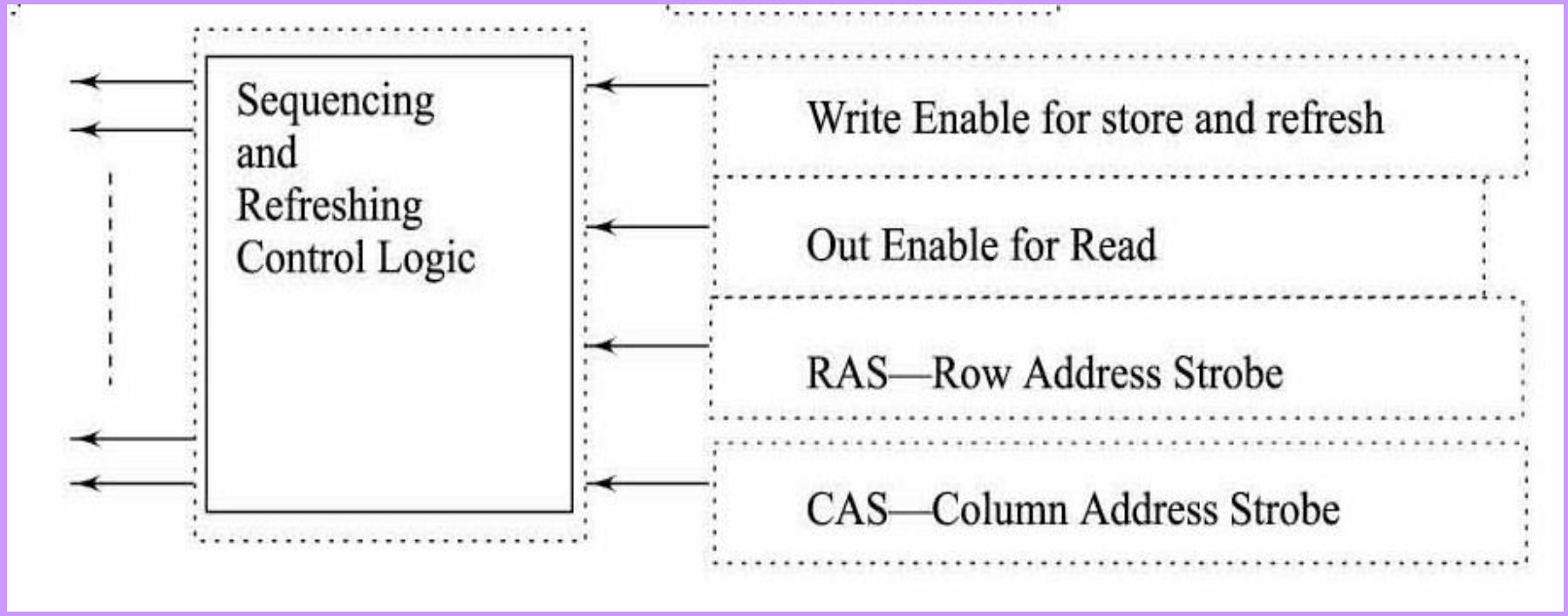
Example of an internal organization for row Address accesses in Normal mode

- 4096 rows × 1024 columns 4M × 8 DRAM

An internal organization in 4M × 8, and row and column decoding by RAS and CAS signals



Sequencing and refresh control logic



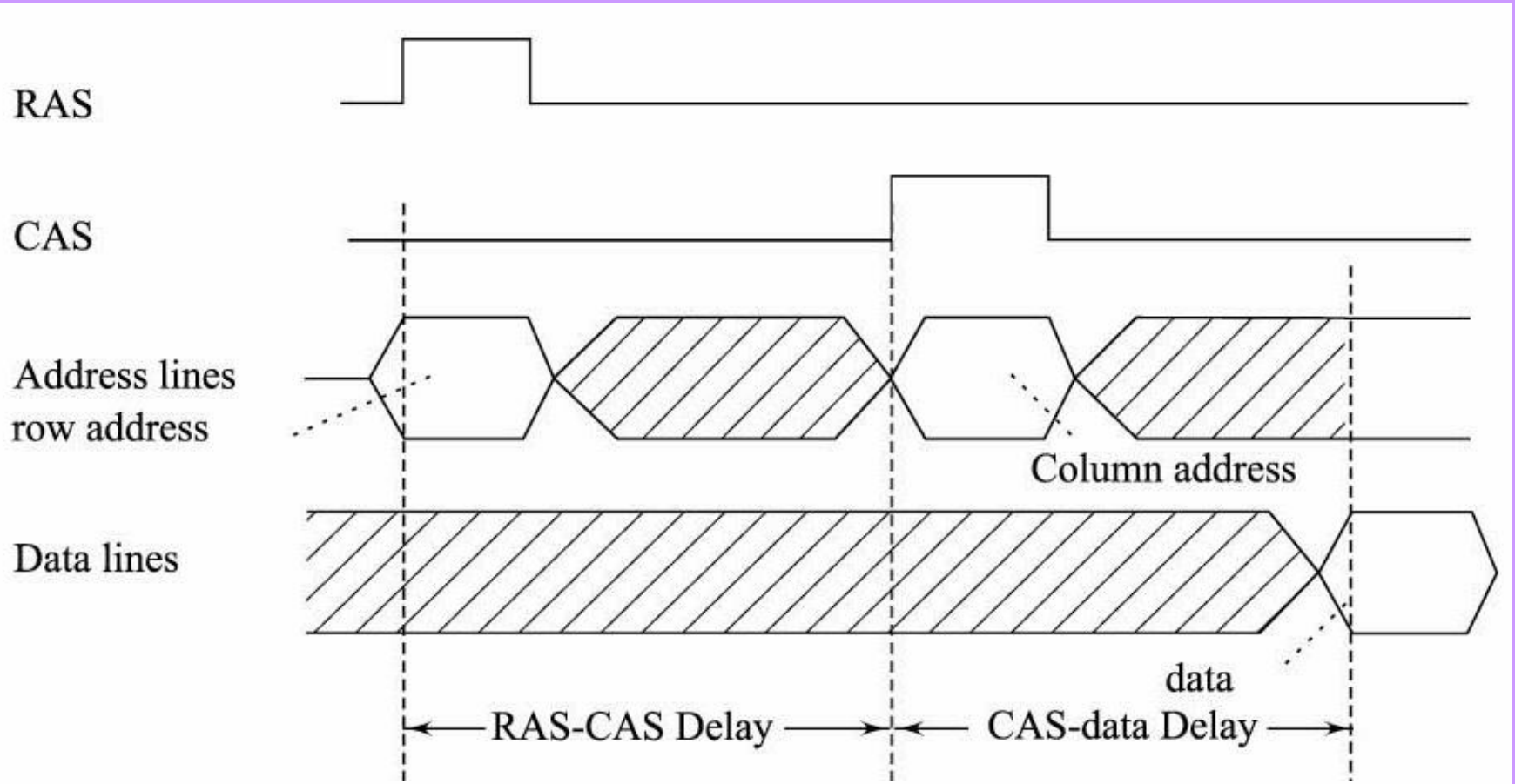
Decoding and RAS and CAS signals

- Row addresses and column addresses decoded
- Row access signal and column access signals, called RAS and CAS
- The RAS (row address strobe) signal when a row address being sent
- The CAS (column address strobe) signal when a column address being sent

Drain Access Timings

- Row address between $t0 - \Delta t0$ and $t1 + \Delta t1$
- Column address between $t3 - \Delta t3$ and $t4 + \Delta t4$

DRAM Read access (both RAS and CAS deactivate before start of each new read and write)



Total DRAM Read Time

- The total time to read the DRAM is the sum of the RAS-CAS delay and the CAS-DATA delay

Write Operations

- Write operations have similar timings, but the DATA lines to be written is generally driven on the data pins at the same time as the column address

Sending the address to the DRAM in two parts

- Reduces the number of address pins at DRAM chip because the same pins can be used for the row and column addresses
- Doesn't significantly increase the access time of the DRAM, because the row address selects the row of the bit cell array whose contents are driven on the bit lines, while the column address selects which bit line is driven to the output

Column Address

- Therefore, the column address isn't needed by the DRAM until the bit cells have driven their outputs onto the bit lines, so sending it to the DRAM after the row address doesn't increase the access time

Weakness of the asynchronous normal mode memory chip design

- An entire row's contents sent to the multiplexer during each operation, but only 1 bit out of the row is actually sent to the output

Asynchronous DRAM

- DRAM which does not provide for DRAM access using clocked latch
- Without clocked sequencer for SDRAM (Synchronous) pipelined access mode
- Does not provide increase in throughput by pipelining and by interleaving

Summary

We learnt

- Asynchronous access DRAM
- Access cycles and Time computation in Asynchronous DRAM in normal mode

End of Lesson 06 on

Asynchronous Dynamic RAMs (DRAMs) and Access cycles and access time in Asynchronous DRAM in normal mode