Chapter 08: The Memory System

Lesson 05:

SRAM and DRAM Memory chips and their internal Organisation

Objective

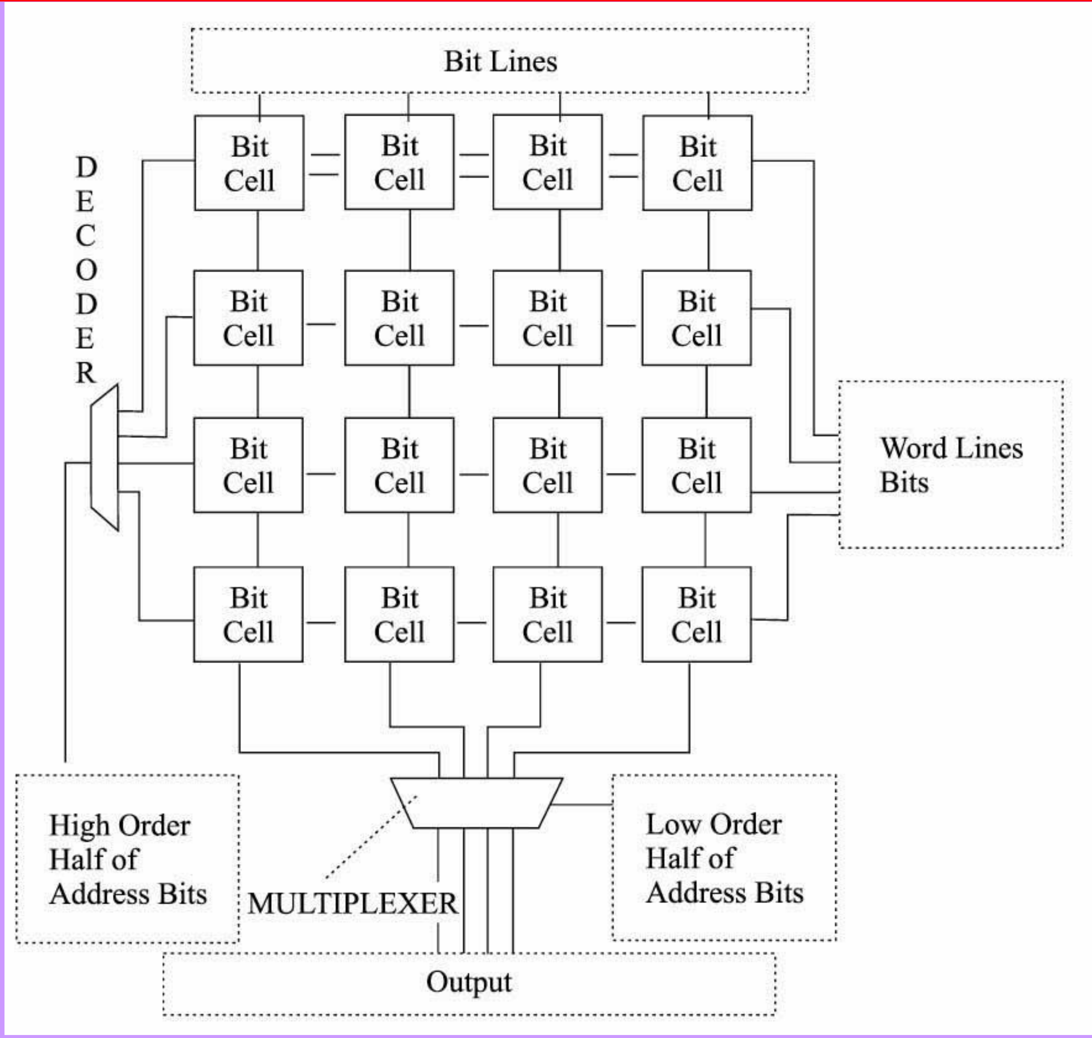
- Understand the process of read, write into bit cells
- Learn Semiconductor Main Memories - SRAM and DRAM

Memory Chip Organisation

Memory Chip

- Same basic structure in SRAM and DRAM memory chips
- Data stored in a rectangular array of bit cells
- Each cell holds 1 bit of data

Memory chip organisation



MUX (multiplexer) during read

- A circuit which at an instance selects from the number of inputs and gives one of the input in the output (for example, during read)
- Which one that depends on input-address or channel selected for the output

MUX Logic during write

- A MUX (multiplexer) function as demultiplexer logic circuit (for example, during write), when at an instance it selects one line from the number of output lines and gives its input at the line

Decoder Logic

- A logic circuit, which at an instance activates one of the output line, which it selects as per the input-address lines

Accesses of bit cells in memory

Read Operation

- Half of the address bits to be read (generally the high-order bits) is fed into a decoder
- The decoder asserts (drives high) a word line corresponding to the value of its input bits
- Causes all of the bit cells in the corresponding row to drive their values onto the bit lines that they are connected to

Read Operation

- The other half of the address bits (generally the low-order bits) is then used as the addressed bit-select input to a multiplexer that selects the appropriate bit line and drives its output onto the output pins of the chip

Write (store) Operation

- To store data on the chip, the same process is used as for the read, except the value to be written is driven on the appropriate bit line and written into the selected bit cell

Number of Output Bits on Access

- Most memory chips generate more than 1 bit of output
- This is done either by building several arrays of bit cells, each of which produces one bit of output, or by designing a multiplexer that selects the outputs of several of the bit lines and drives them on the chip's outputs

Speed of a Memory Chip Access

- Determined by a number of factors, including the length of the bit and word lines and how the bit cells are constructed
- Longer bit and word lines have higher capacitances and resistances, so it takes longer to drive a signal on these wires as their lengths increase

Modern memory chips

- To lower the capacitances and resistances to reduce the access latency— constructed out of many small arrays of bit cells to keep the word and bit lines short

Effect of Techniques used in constructing the bit cells

- Speed of the memory chip— because they affect how much current is available to drive the output of the bit cell onto the bit lines
- The current determines how long it takes to propagate the bit cell’s output to the multiplexer
- SRAM bit cells drive much more current than DRAM bit cells
- SRAMs tend to be much faster than DRAMs

SRAMs and DRAMs

SRAMs typically much faster than DRAMs

- In SRAMs, an active device (the inverter) drives the value stored in the bit cell onto the bit line and inverted bit line

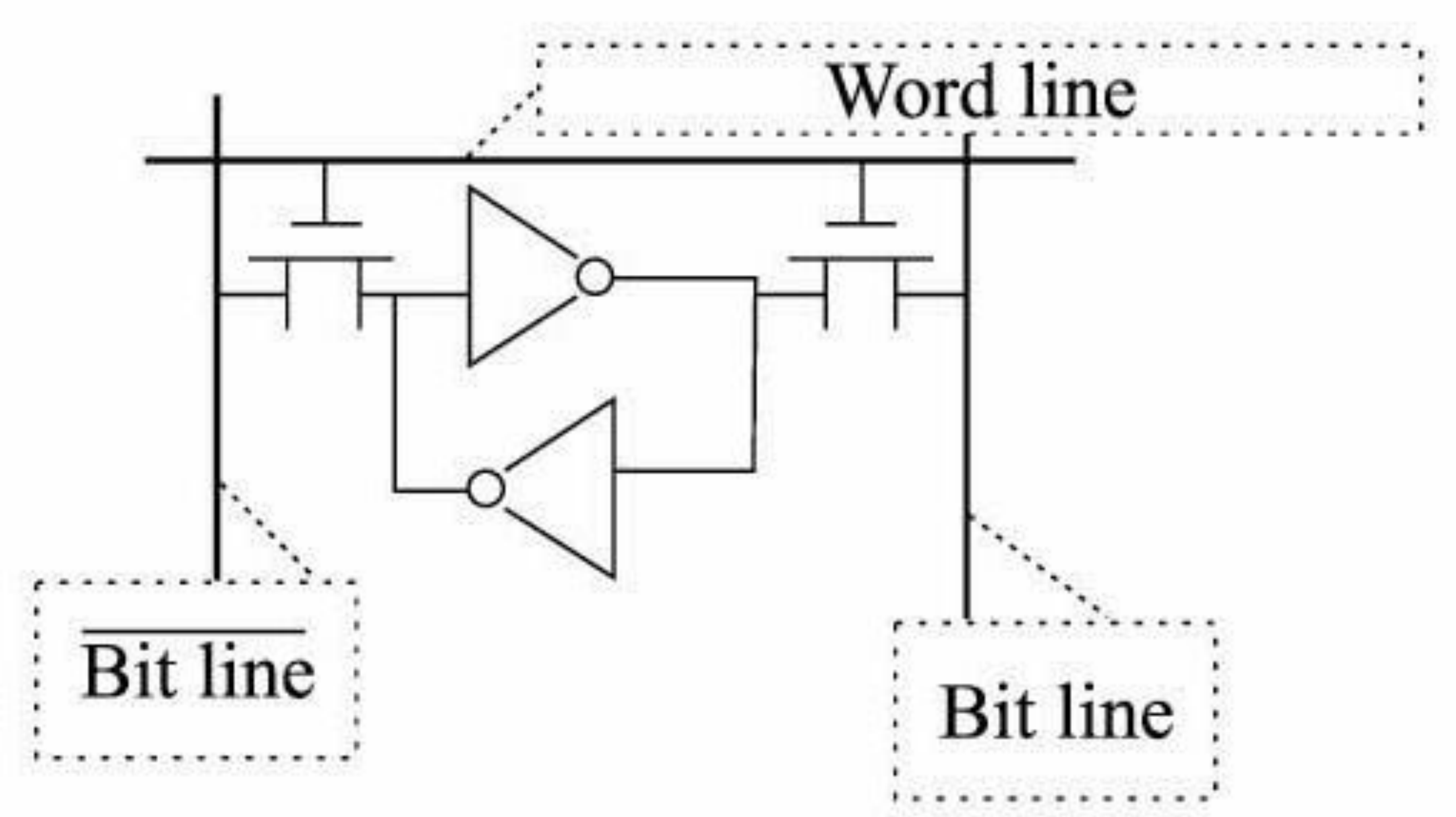
DRAMs typically slower than SRAMs

- In DRAMs, the capacitor is connected to the bit line when the word line is asserted, which is a much weaker signal than the one produced by the inverters in an SRAM bit cell
- Thus, it takes much longer for the output of a DRAM bit cell to be driven onto its bit line than it takes for an SRAM bit cell to drive an equivalent bit line

Main difference between SRAMs and DRAMs

- Bit cells construction
- Core of an SRAM bit cell consists of two inverters connected in a back-to-back configuration
- Core of an DRAM bit consists of a transistor and capacitor

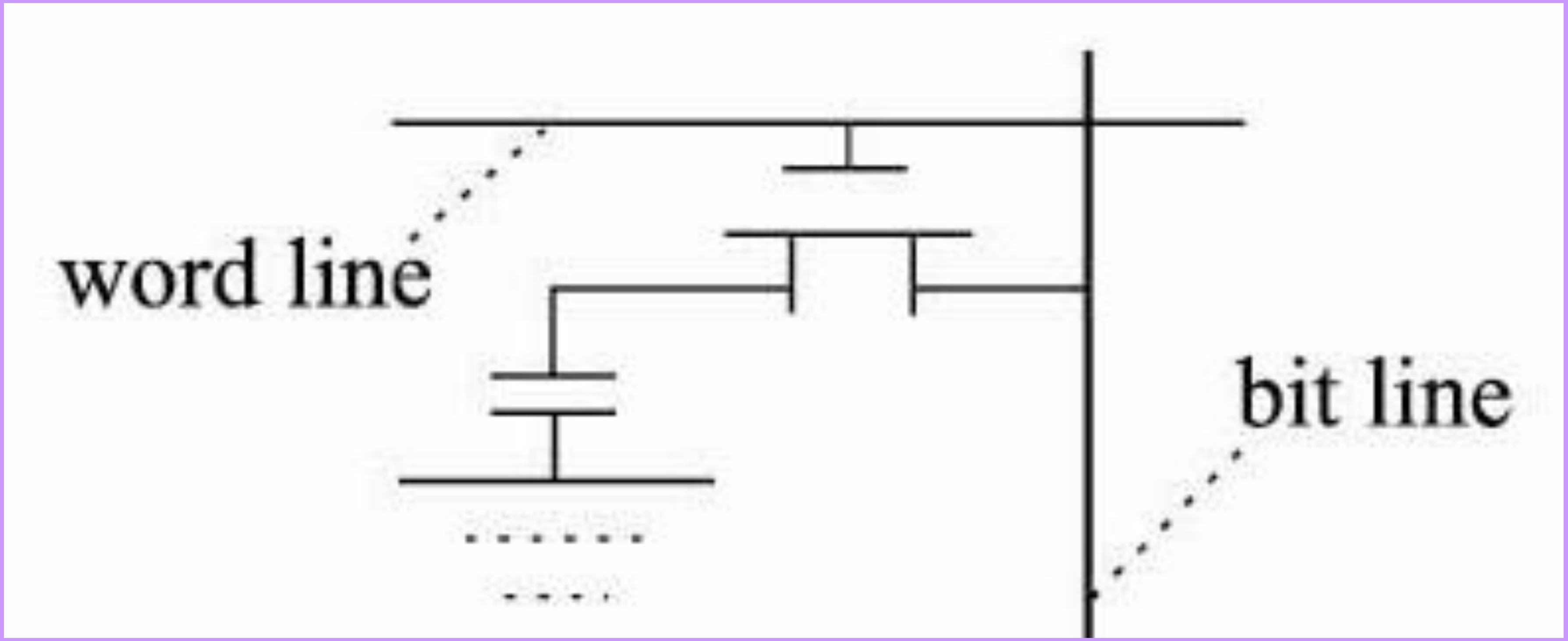
Core of an SRAM bit cell



SRAM

- Once a value has been placed in the bit cell, the ring structure of the two inverters will maintain the value indefinitely because each inverter's input is the opposite of the other's
- This is the reason why SRAMs function as the static RAMs; the values stored in the RAM remain there as long as power is applied to the device

Core of a DRAM bit cell



DRAMs

- Loses their stored values over time, which is why they are known as *dynamic* RAMs

SRAM smaller capacities than DRAMs much larger capacities

- Assume SRAMs constructed in the same fabrication technology
- SRAMs require many more devices to implement a bit cell
- Each inverter typically requires two transistors, for a total of six transistors in the bit cell
- In contrast, a DRAM bit cell requires only one transistor and one capacitor, which take up much less space on the chip

Reading from SRAM

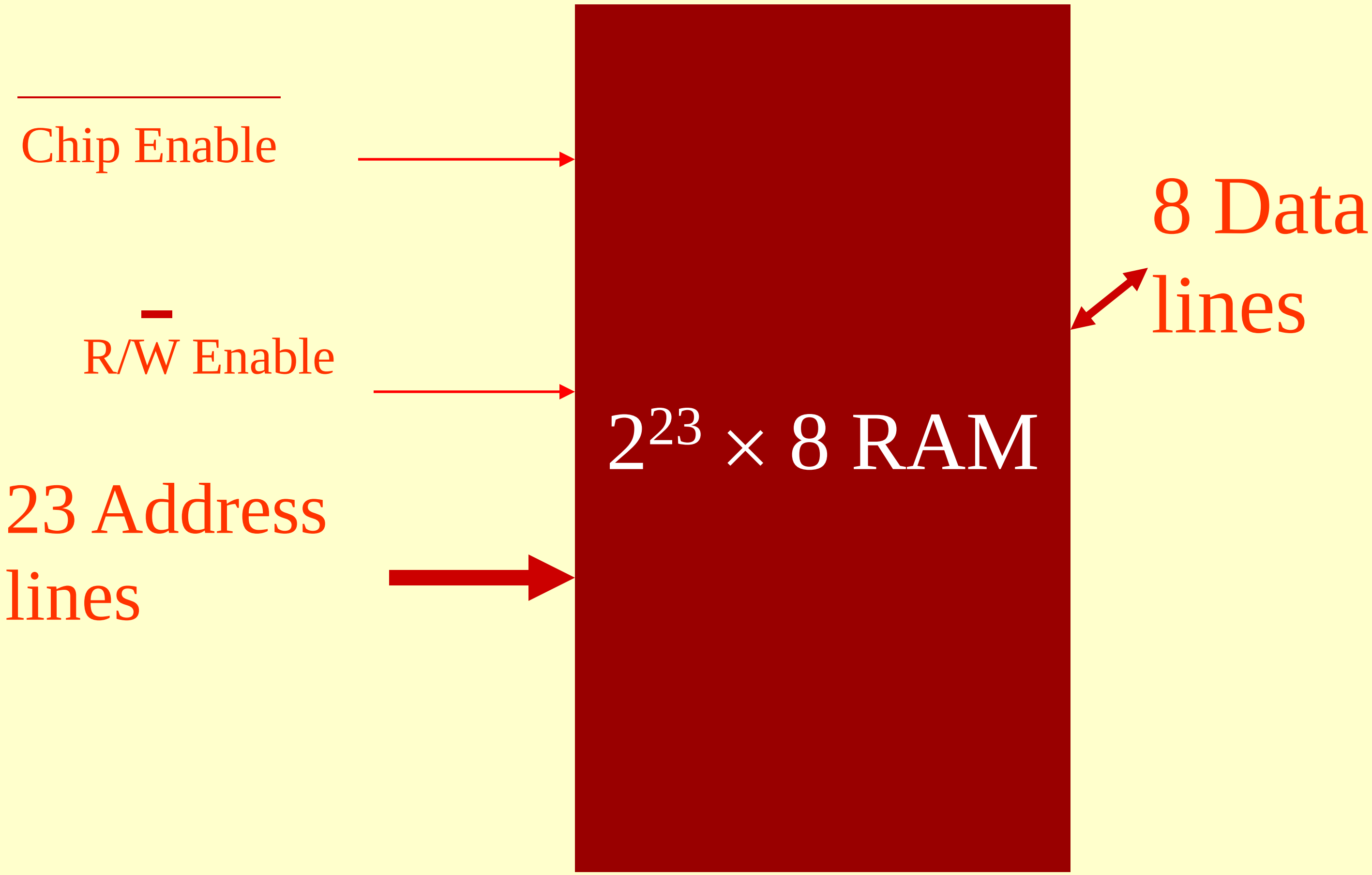
- To read a value from the bit cell, the word line driven high
- Two transistors connects the outputs of the inverters to the bit line and inverted bit line
- These signals can then be read by the multiplexer and sent to the output of the chip

Writing into SRAM

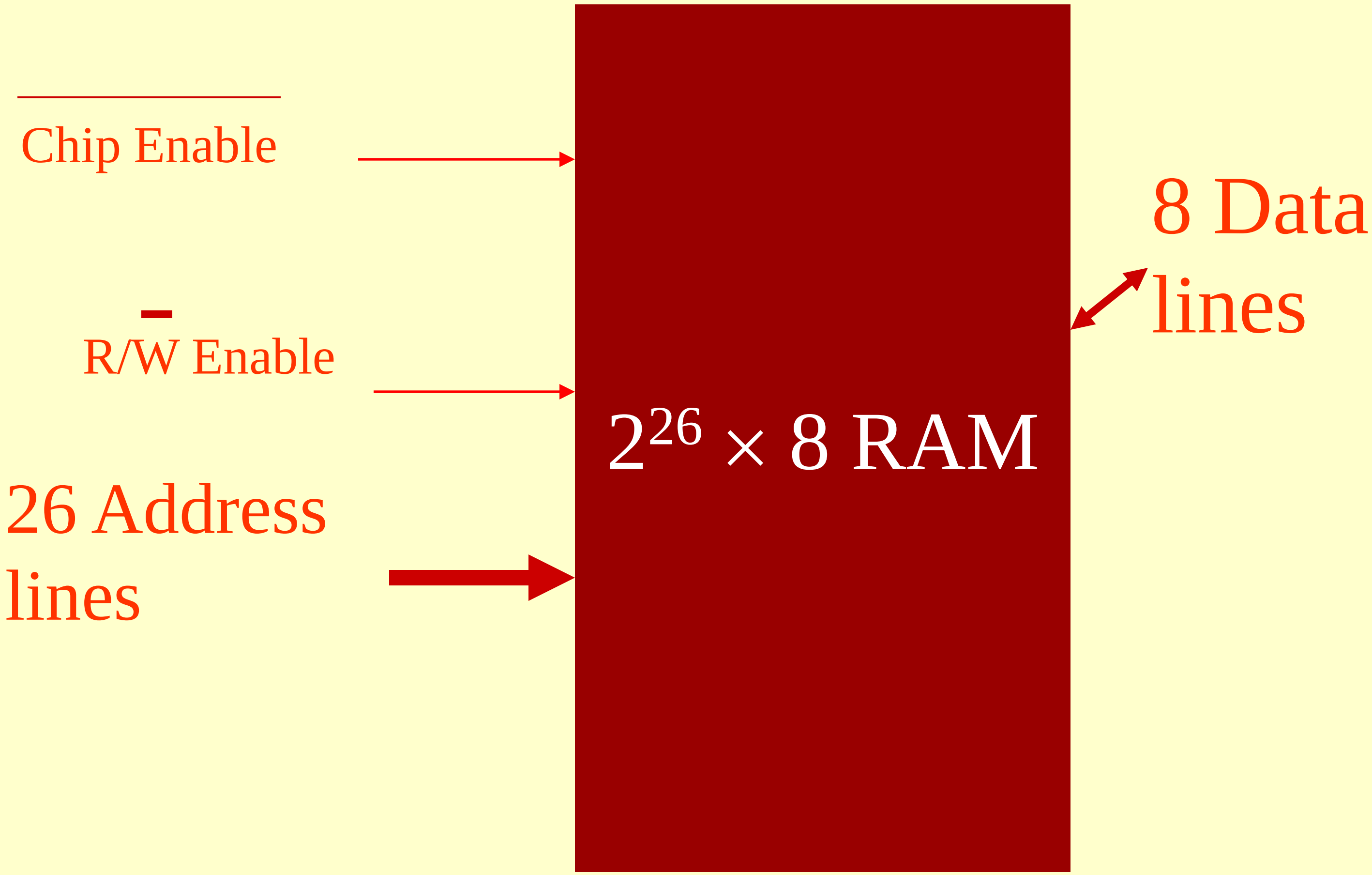
- Writing an SRAM bit cell is accomplished by asserting the word line and driving the appropriate values on the bit line and inverted bit line
- As long as the device driving the bit line is stronger than the inverter, the values on the bit line will dominate the value originally stored in the bit cell, and will be stored in the bit cell when the word line is de-asserted

Memory chip

8 MB RAM


$\overline{\text{Chip Enable}}$
R/$\overline{\text{W}}$ Enable
23 Address lines
$2^{23} \times 8$ RAM
8 Data lines

64 MB RAM

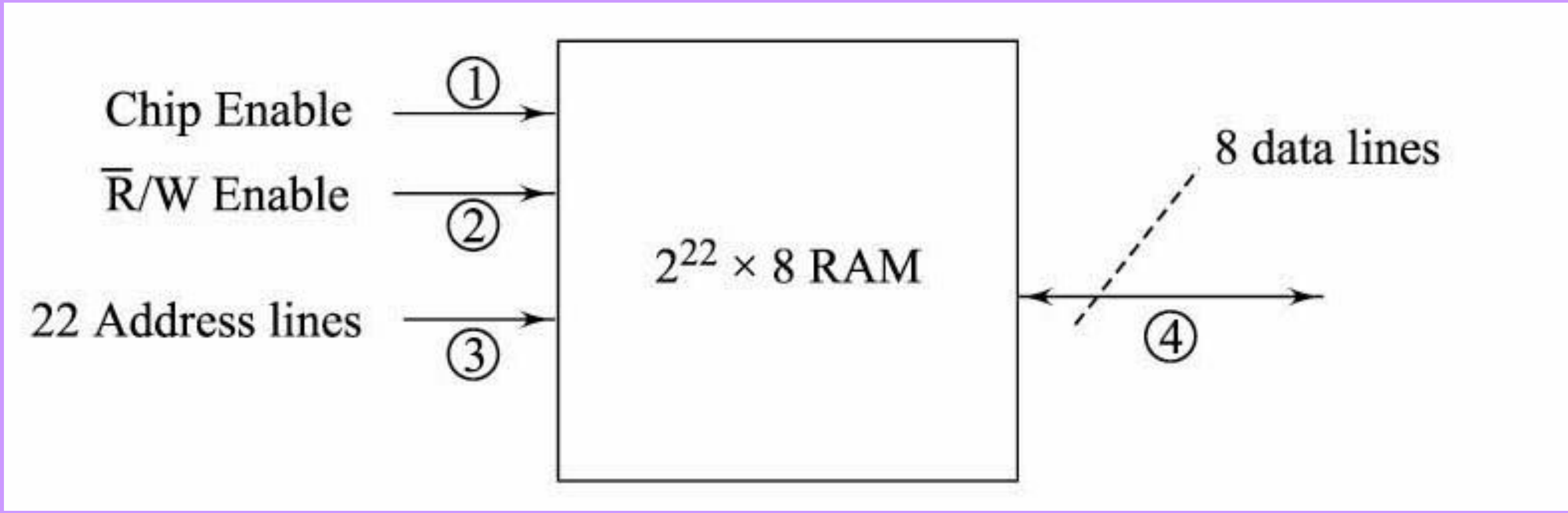

$\overline{\text{Chip Enable}}$
R/$\overline{\text{W}}$ Enable
26 Address lines
$2^{26} \times 8$ RAM
8 Data lines

Bus signals to a Memory chip

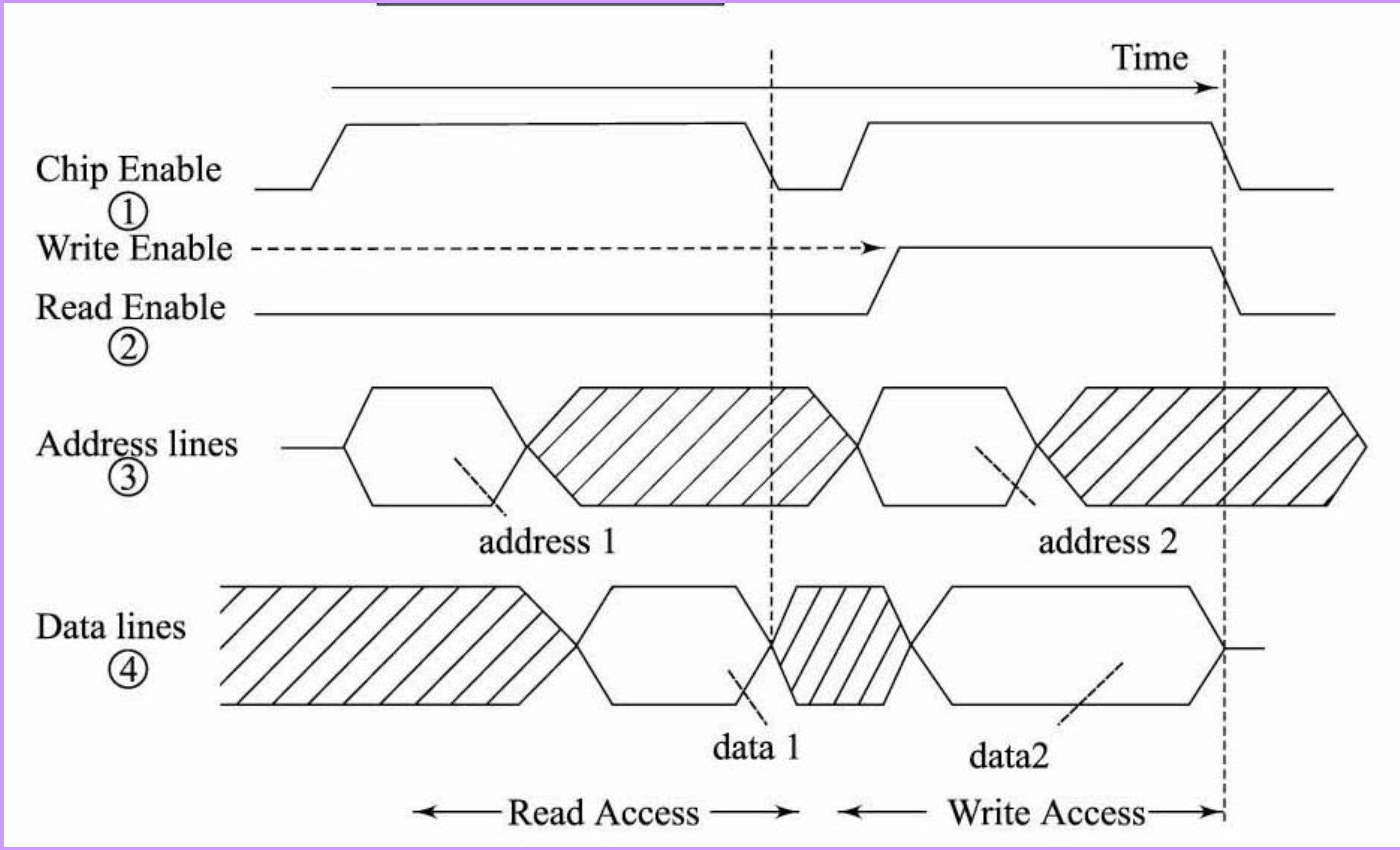
Bus Signals

- t0 to t2 CS enable and t0 + Δt0 to t0 + Δt0 + Δt0' Address Latch enable
- t0 + Δt0 + Δt0' + Δt0'' to t2 – Δt2' RD enable
- t0 + Δt0 + Δt0' + Δt0'' to t2 – Δt2' $\overline{\text{WR}}$ enable
- t0 + Δt0 + Δt0'' to t2 + Δt2'' Address Lines
- t0 + Δt0 + Δt0' + Δt0'' + Δt0''' to t2 –Δt2'' Read at Data Lines
- t0 + Δt0 + Δt0' + Δt0'' + Δt0''' to t2 – Δt2' + Δt2''' Write at Data Lines

$2^{22} \times 8$ SRAM



Read and write



Summary

We learnt

- Understand the process of read, write into bit cells
- Semiconductor Main Memories - SRAM and DRAMs
- Bit cell in SRAM
- Bit cell in DRAM
- Chip signals
- Bus signals

End of Lesson 05 on

SRAM and DRAM Memory chips and their internal Organisation