Chapter 07: Instruction–Level Parallelism– VLIW, Vector, Array and Multithreaded Processors …

Lesson 05:

Array Processors

Objective

- To learn how the array processes in multiple pipelines

Array Processor

Array

- A vector (one dimensional array)
- A set of vectors (multi-dimensional array)
- Array processor — a processor capable of processing array elements
- Suitable for scientific computations involving two dimensional matrices

Array processor

- Array processor performs a single instruction in multiple execution units in the same clock cycle
- The different execution units have same instruction using same set of vectors in the array

Special features of Array processor

- Use of parallel execution units for processing different vectors of the arrays
- Use of memory interleaving, *n* memory address registers and *n* memory data registers in case of k pipelines and use of vector register files

Single instruction on vectors in Array processor

- An array processor has single instructions for mathematical operations, for example, SUM *a*, *b*, *N*, *M*

  a— an array base address

  b— another vector base address

  N— the number of elements in the column vector

  M— the number of elements in row vector

Different execution units

- Same instruction using same set of vectors in the array

Classification of Array Processors

SIMD (single instruction and multiple data) type processor

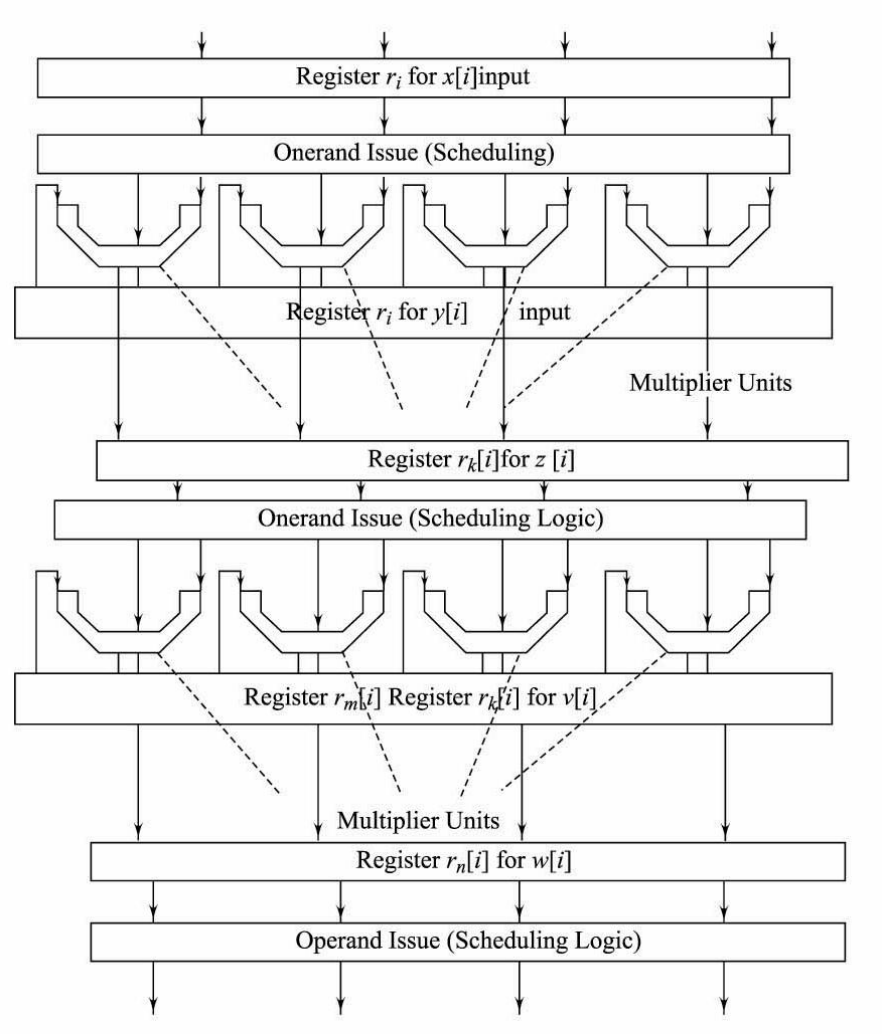
- Data level parallelism in array processor, for example, the multiplier unit pipelines are in parallel Computing x[i] × y[i] in number of parallel units
- It multifunctional units simultaneously perform the actions

Attached array type processor

2. Second type attached array processor

- The attached array processor has an input-output interface to a common processor and another interface with a local memory
- The local memory interconnects main memory

SIMD array processor



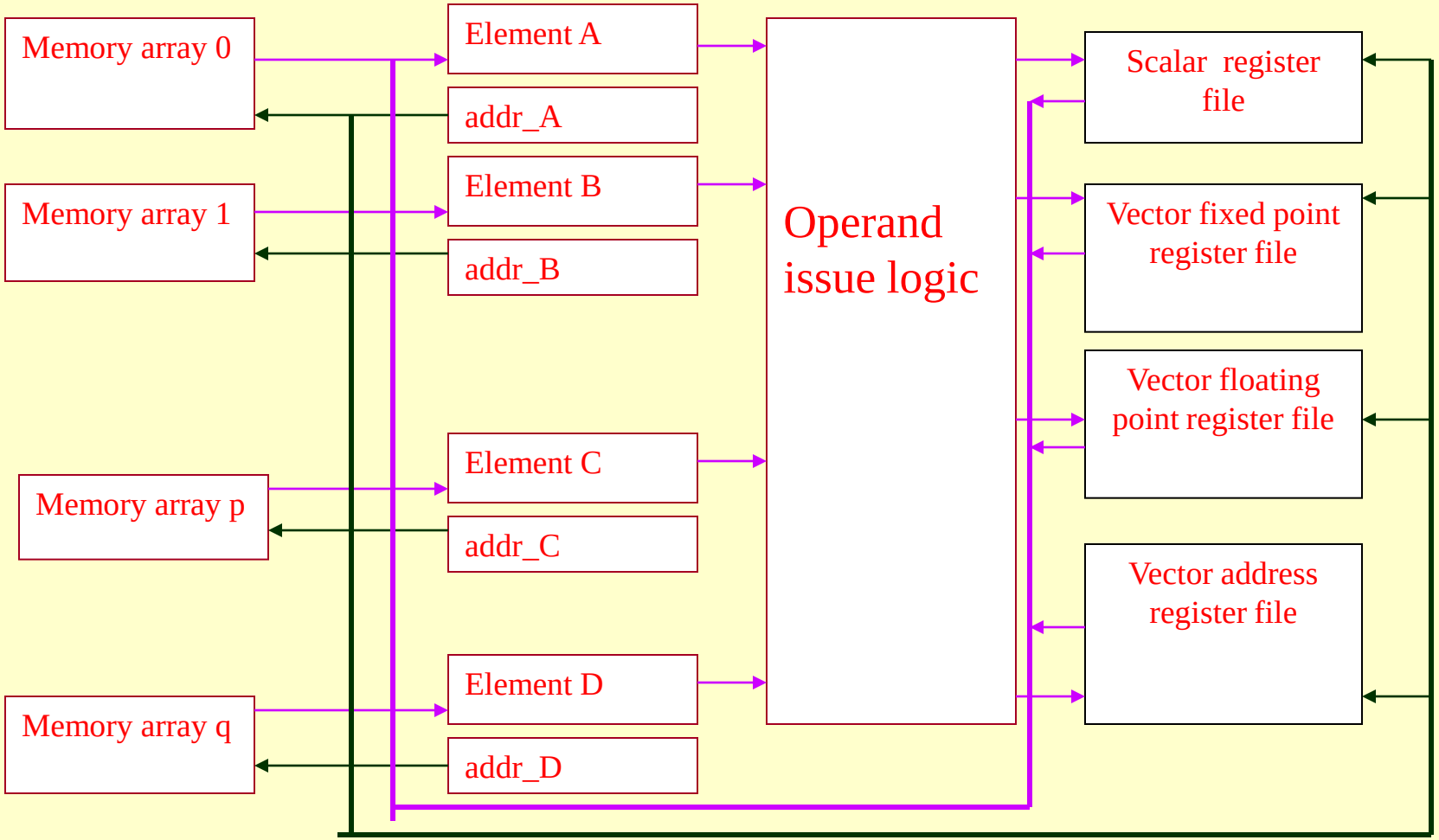
Multiplication operation for each vector element in one dimensional matrix

- Needs n sums of the multiplicands
- $K = \sum I(r).\ J(r)$ for $r = 0, 1, 2, \ldots,$ up to $(n-1)$

Multiplication operation for each vector element in two dimensional matrix

- Needs n sums of the multiplicands
- $K(p, q) = \sum I(\text{p, r}).\ J(\text{r, q})$ for r = 0, 1, 2, …, up to (n–1)
- Where p = 0, 1, 2, …, up to (n–1)
- q = 0, 1, 2, …, up to (n–1)
- Array processor processes these in parallel

Interleaved memory arrays interconnections with the processor



Word addresses of arrays A and B at input and element addresses array C as output

- From three execution units in eight clock cycles in an array processor
- Figure 7.12

Summary

We Learnt

- Array processor
- SIMD processor
- Attached processor
- Memory interleaving in register files by operands issue logic

End of Lesson 05 on

Array Processors