Chapter 06: Instruction Pipelining and Parallel Processing

Lesson 13:

Dynamic Hardware Branch Prediction

Objective

- Understand the advantage of branch prediction dynamically

Hardware for pre-calculation of Branch Address

Pre-calculation of Branch

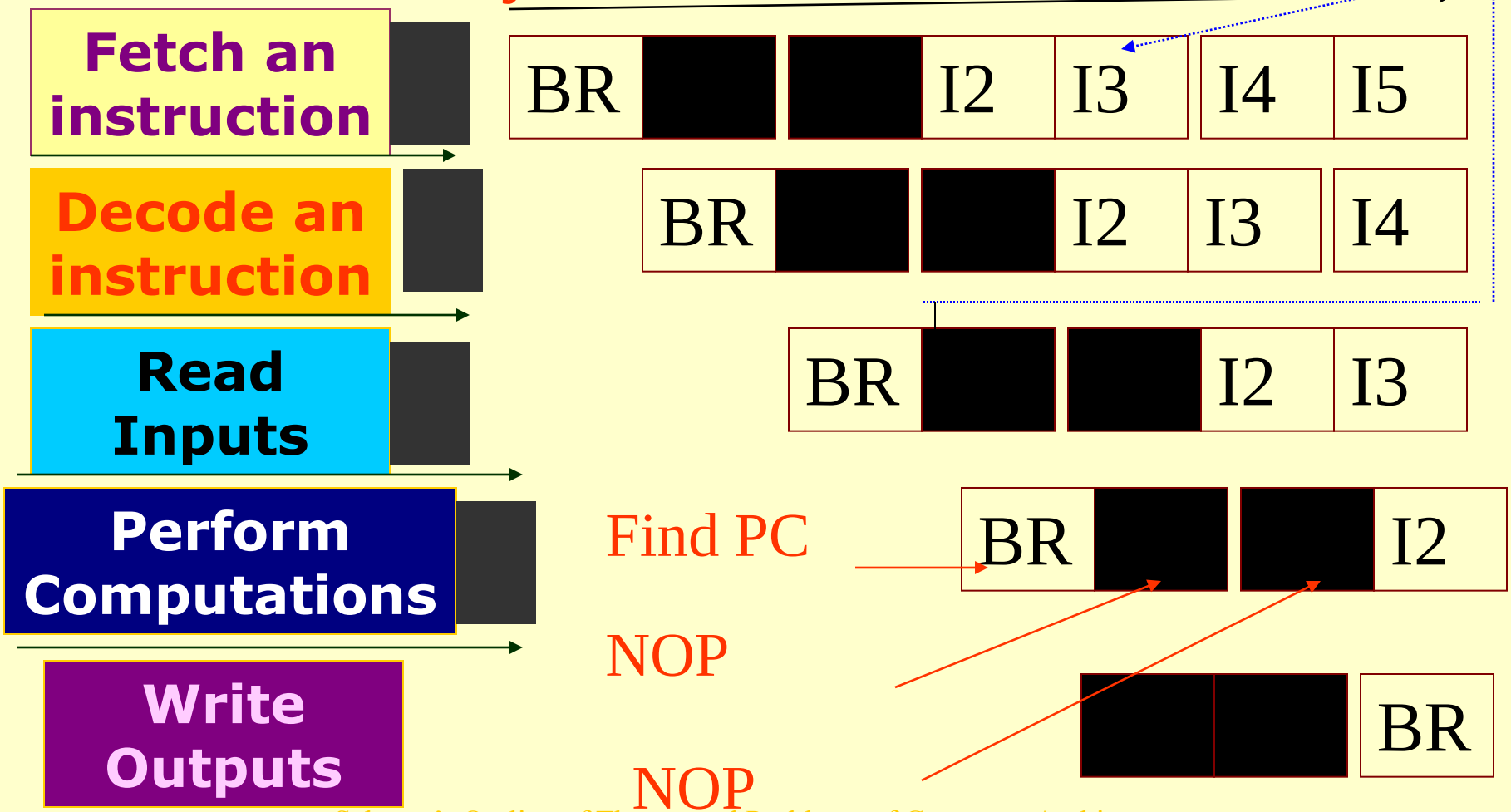
- Add hardware to allow the result of a branch instruction to be computed earlier in the pipeline

Example of Pre-calculation of Branch

- If the pipeline computed the next value of the PC in the register read stage instead of the execute stage, the branch delay would be reduced to three cycles
- Only two bubbles if PC value forwards to fetch stage

Four Cycles for New PC value and 2 bubbles

Seven Clock Cycles



Branch Prediction

Condition Branch Instruction control hazard

- Dependency of the PC on the result causes delay (branch penalty) because pipelined instruction has to wait till write-back of the PC finishes at the write-back stage

Branch Prediction

- A powerful technique is there to predict the value of PC, which then proceeds to execute I_n, I_{n+1}, I_{n+2}, I_{n+3}, …., the new instruction path as per the condition at cond field
- If the prediction is incorrect, then the path cancels and branch penalty imposes; else the prediction improves the performance

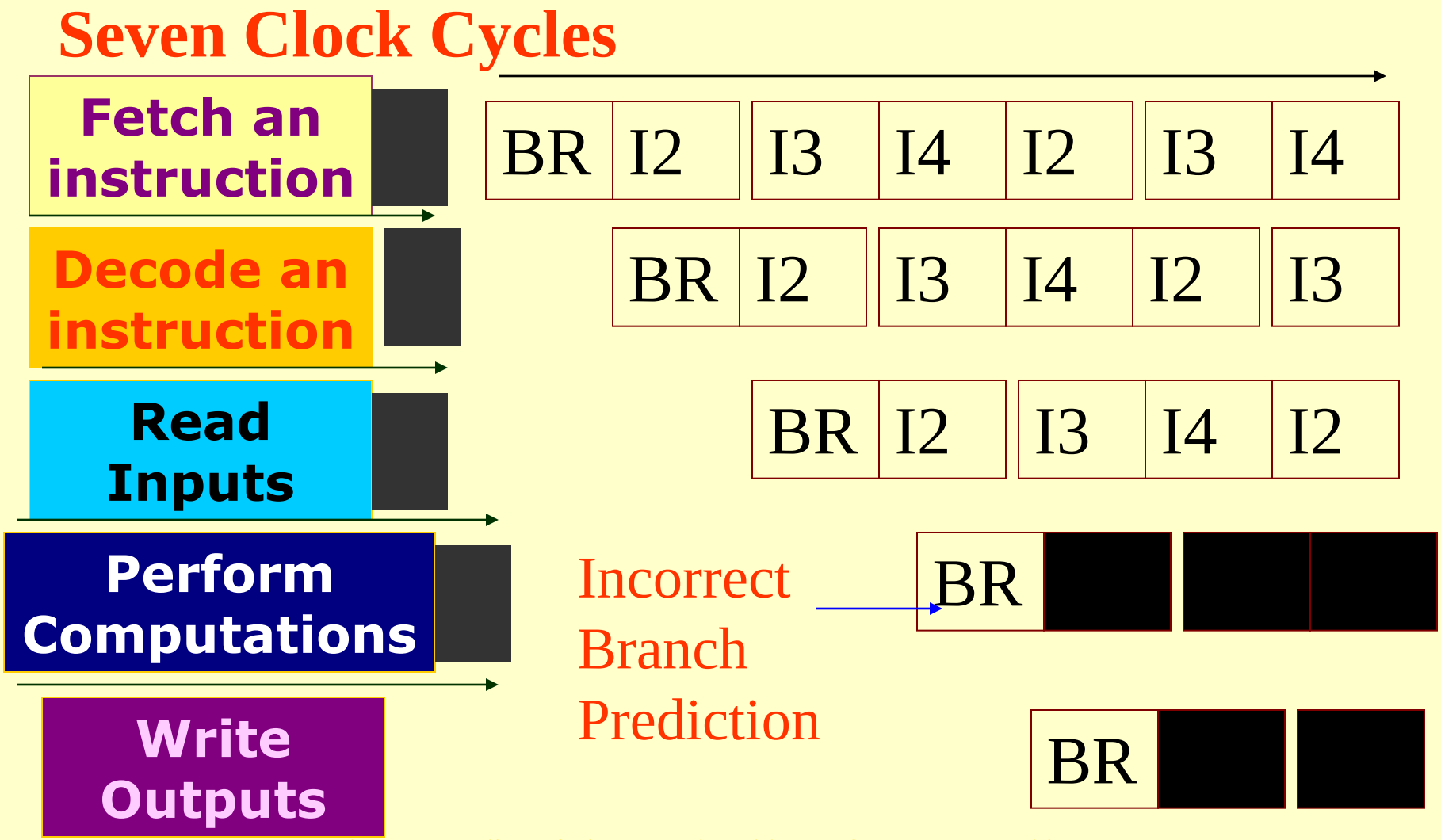
Branch Prediction

- Add hardware that predicts the destination address of each branch before the branch completes
- Allowing the processor to begin fetching instructions from that address earlier in the pipeline

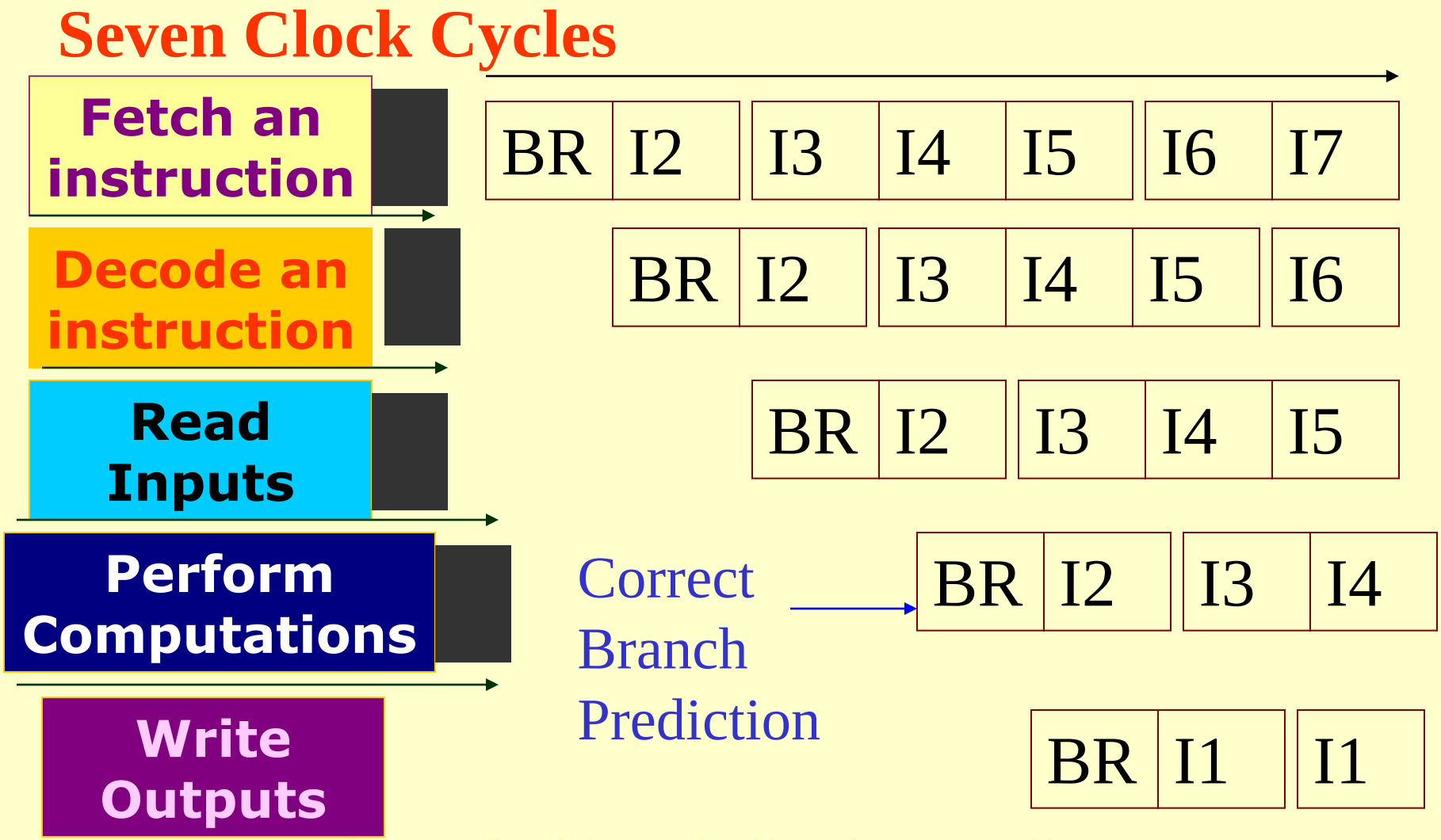
SuperSparc processor

- Uses the branch-prediction technique
- Accurate predictions possible
- A dynamic hardware predicts the PC and thus the instruction path

Seven Clock Cycles Incorrect Branch Prediction for I2



Seven Clock Cycles without correct Branch Prediction for I2



Branch Prediction

- A dynamic hardware to predict the PC and thus the instruction path

Dynamic Branch Prediction and use of I-bit

Dynamic Prediction Hardware

- Let us assign a control prediction bit p to the instruction I_n when it first executes
- Processor hardware uses p bit with I_n to predict on subsequent use of I_n

Loops Handling with Dynamic Prediction Hardware

- After the first assignment of p bit, the loop back address will be predicted and will not have any instruction that does not have the branch penalty
- A correct prediction sets a bit $q = 1$ when $p = 1$

p-and q-bits Bit

- As long as *q* remains 1, the prediction is correct and *p* remains 1
- When prediction is incorrect, the *q* resets to 0 and it forces *p* also 0
- The processor now follows the path before the prediction

Dynamic Branch Prediction and use of branch target buffer

Use of branch target look ahead buffer (BTB)

- Let us assume that the hardware has a branch history table

Branch History Table Row

- Instruction address
- predicted branch target address
- number of times prediction and number of times succeeded, made, and predicted correctly

Instruction I_n

- Request to instruction I_n sent to instruction cache as well as to BTB

Use of branch target look ahead buffer (BTB)

- If I_n matches an entry in BTB, then the predicted address is used and the field for the number of times prediction updates
- After execution of the instruction, target address updates

Use of branch target look ahead buffer (BTB)

- Also if prediction succeeds, the field for success is updated by increasing the value
- If it fails, then by decreasing the value.

Summary

We Learnt

- Advantage of branch prediction
- Dynamic branch prediction
- Use of instruction bits p and q, branch table low in branch target look ahead buffer

End of Lesson 13 on

Dynamic Hardware Branch Prediction