Chapter 06: Instruction Pipelining and Parallel Processing

Lesson 07: Overcoming Hazard by Result Forwarding (Bypassing)

Objective

• Learn how the data dependency effect overcome by result forwarding

Overcoming Hazard **by** Result Forwarding

Reducing Data dependency Effects

• In addition to the conventional write-back path at last stage of the instruction, connections are added that send the output of the execute stage directly to the input of the execute stage and to the register read stage

Result Forwarding Mechanism

• Due to result forwarding from fourth stage (compute) to third stage (read), only two-cycle stall would suffice

Forward paths for result forwarding (bypass) path



Pipeline stall in cycle 6 between SUB and MUL

	Cycle						
	1	2	3	4	5	6	7
Fetch→	ADD	SUB	MUL	ASH	OR	OR]
	r_1 ,	<i>r</i> 4,	r ₈ ,	$r_{5},$	$r_{10},$	$r_{10},$	
	r_2, r_3	<i>r</i> ₅ , <i>r</i> ₆	r_2, r_1	r_2, r_1	$r_{11},$	r_{11}, r_4	
		ADD	SUB	мш	ASH	ASH	OR
Decode —		r_1	r ₄ ,	rs.	r5.	r5. r2.	r_{10}
		r_2, r_3	r_5, r_6	r_2, r_1	r_2, r_1	r_1	r_{11}, r_4
			ADD	SUB	MUL	MUL	ASH
Read —		—	r_1 ,	r_4 ,	$r_{8},$	<i>r</i> ₈ ,	r ₅ ,
			r_2, r_3	r_5, r_6	r_2, r_1	r_2, r_1	r_2, r_1
Execute				ADD	SUB	(huh	MUL
			≻	r_1 ,	r_4 ,	ble)	$r_{8},$
			i i	r_2, r_3	r_5, r_6	010)	r_2, r_1
Write back———				:	ADD	SUB	
			:	\mapsto	r_1 ,	r_4 ,	(bubble)
			1	:	r2, r3	r5, r6	

ADD in Cycle 4 and SUB in Cycle 7

- The result of the ADD instruction computed in the execute stage of the pipeline in cycle 4
- But the SUB instruction is unable to issue until cycle 7 because the result of the ADD is not written into the register file until cycle 5, allowing the subtract to read it on cycle 6 only

ADD in Cycle 4 and SUB in Cycle 7

• If the result of the ADD could be sent to the subtract instruction directly, without going through the register file, the subtract could issue on cycle 5 without any pipeline stalls

Result forwarding (bypassing) in Virtually all pipelined processors

 Result forwards from the execute stage(s) directly to the instructions in the previous stages of the pipeline

Result forwarding (bypassing)

• The instruction latency of non-branch instructions in a pipeline with bypassing is equal to the number of execute stages in the pipeline, because the output of an instruction is not computed until it completes the last execute stage, but an instruction's inputs are required when it enters the first execute stage

Result forwarding (bypassing) in case of branch operation

- Bypassing does not usually improve the latency
- The results of branch instructions are not written into the register file

Summary

We learnt

• Result forwarding from last of the execution stages to previous reduces the dependency effects

End of Lesson 07 on Overcoming Hazard by Result Forwarding (Bypassing)