Chapter 05: Basic Processing Units … Control Unit Design

Lesson 16:

Horizontal and Vertical organisation of Microinstructions

Objective

•Learn how to group the microoperations to use one control signal for the group

• Understand Horizontal and vertical organization

• Learn how to reduce control fields in memory storage by use of MUXs in the output word form control memory

Grouping of the Control Signals in Microinstruction

Simplification

- Group a set of control signals c0, c1,.. by a single control signal C and thereby reduce the signals needed from the output of control memory
- Grouping of the Control Signals in Microinstruction
- Reducing Control Signals by Use of MUXs

Grouping

- Group a set of control signals *c*0, *c*1,.. by a single control signal *C*
- Reduce the signals needed from the output of control memory

Group of signals

- Group of signals for fetching an instruction at address I placed in PC and incrementing the PC for the next instruction, can be grouped by two control signals $C0$ and $C1$
- $C0$ is for microoperations for instruction fetch
- $C1$ is for microoperations memory data read from an address placed at TEMP with load of data from memory

Grouped Control Signal for Microinstructions *C0* for fetch instruction at address *a*

- PC $\rightarrow$ MAR
- Branch for implementing PC $\leftarrow$ PC + 4
- ALE active
- MEMRD activate
- M(*I*) $\rightarrow$ MDR
- MEMRD deactivate

Grouped Control Signal for Microinstructions *C1* for fetch data at address a_j

- TEMP $\rightarrow$ MAR
- No action
- ALE active
- MEMRD activate
- M(*TEMP*) $\rightarrow$ MDR
- MEMRD deactivate

Two Bits C1C0 in Microinstructions at address a_j

- 00: No fetch or store operation
- 01: Fetch
- 10: fetch data

- A sequential circuit connected to $C0$ and $C1$ output from control memory can implement the operations in fetch instructions and fetch data into MDR
- Between addresses a_{j+1} and a_{j+5}, the microinstructions not needing the MAR, MDR, and external buses can now be stored at the control memory

Horizontal Organisation of Microinstructions

Horizontal organisation

- No encoding of control signals in control memory
- When the control signals in a microinstruction are stored in control memory without encoding then the number of storage bits at each address becomes too large

Horizontal organisation in a processor with a processor

- 32 storing-units—IR, 16 registers (*r*0 to *r*15), MDR, MAR, PC, Offset, Temp1, Temp2, *X*, *Y*, *Z*, status flags register SR, stack pointer (SP), and four MUXs, each with a channel select bits register

Horizontal organisation in a processor with a processor

- Total 28 units each with two control signals, one for input and other for output, and four with one control signal each
- Total number of control signals are $28 \times 2 + 4 = 60$

Horizontal organisation

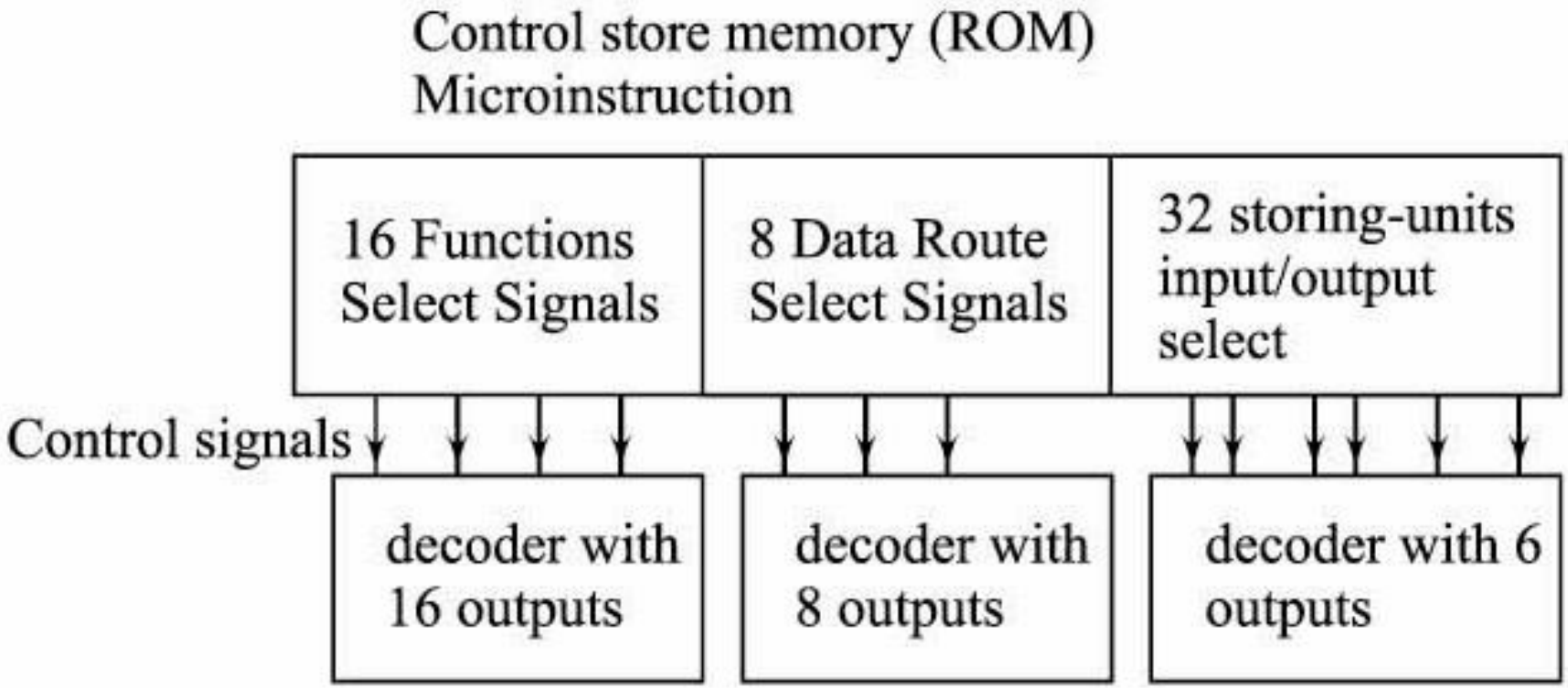
- Now assume sixteen select functions—data transfer, add, sub, …. , which need 16 control signals
- Now assume eight data routes select the control signals
- The total number of control signals becomes 60 + 16 + 8 = 84

Vertical Organisation of Microinstructions

Simplification

- Reducing control fields in memory storage by use of MUXs in the output word form control memory

Three fields in a microinstruction when the control signals encoded in vertical memory organization



Encoding of control signals at control memory address

- When the control signals in a microinstruction are stored in control memory with encoding, then the number of storage bits at each address can be reduced as per the design
- A design selects how many bits to encode out of the needed ones and how many groups of the storing units connect the MUXs

Encoding of control signals at control memory address

- Consider in a processor thirty two ($=2^6$) storing-units
- Suppose each unit is designed independently with no MUX in between
- Then six bits can encode up to 26 storing units controlling signals

Encoding of control signals at control memory address

- The sixteen select functions encode by 4-bits
- The eight data routes encode by 3-bits
- The total number of output word bits at control memory reduces to 6 + 4 + 3 = 13

Summary

We Learnt

- Use of horizontal organization require large number of control bits
- Encoded fields in control memory microinstruction in Vertical organisation of Microinstructions
- Uses of MUXs in Vertical organisation of Microinstructions

End of Lesson 16 on

Horizontal and Vertical organisation of Microinstructions