Chapter 05: Basic Processing Units … Control Unit Design Organization

Lesson 13:

Hardwired control

Objective

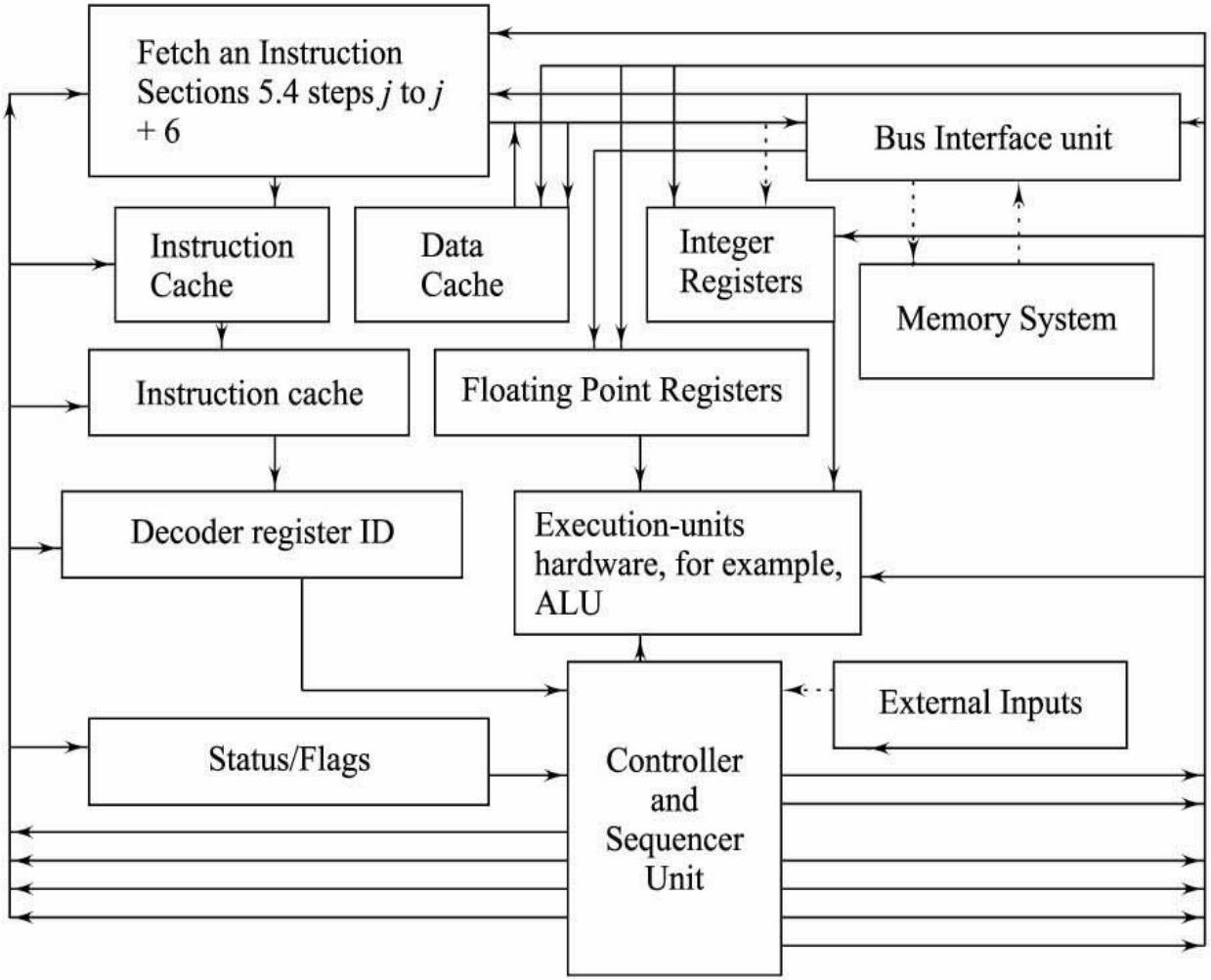
- Understand the design of hardwired control unit to generate all sequences of the control signals
- Learn how an encoder outputs the control signals at each step and generates sequence by hardware from the start of count 0 to the end state
- Learn that encoder circuit outputs the control signals for given inputs from ID, status flags and sequence counter in the hardwired control

Complete Processor

Complete Processor

- Consists of an instruction fetch unit, instruction cache, data cache (including write back cache), bus interface unit, integer register file and floating-point numbers register file; registers IR, ID, MDR, MAR, PC, SP, and other storing units, and MUX units, execution unit, and control unit

Complete Processor



Hardwired Control Unit

Hardwired Control Unit

- The steps required for performing an arithmetic or logical operation, for fetching a word from memory, or for storing a word in memory
- Performed sequentially changing from one step to another
- A control unit required implements the steps

Hardwired Control Unit

- For n sequences of steps, assume that the states are changed in eac step from one state to the next from S_0 to S_{n-1}
- At each state, the set of outputs, $O_{i,0}$ to $O_{i,\ m-1}$, depend on the current states and inputs, I_0 to I_{x-1}

Hardwired Control Unit generating states by its circuit based on Moore state machine

- A set of outputs for the given set of inputs, assuming that the control unit is generating states by its circuit, which is based on Moore state machine concept
- Moore state machine concept is that each output signal $O_{i,0}$ to $O_{i,\, m-1}$ depends on the current state only

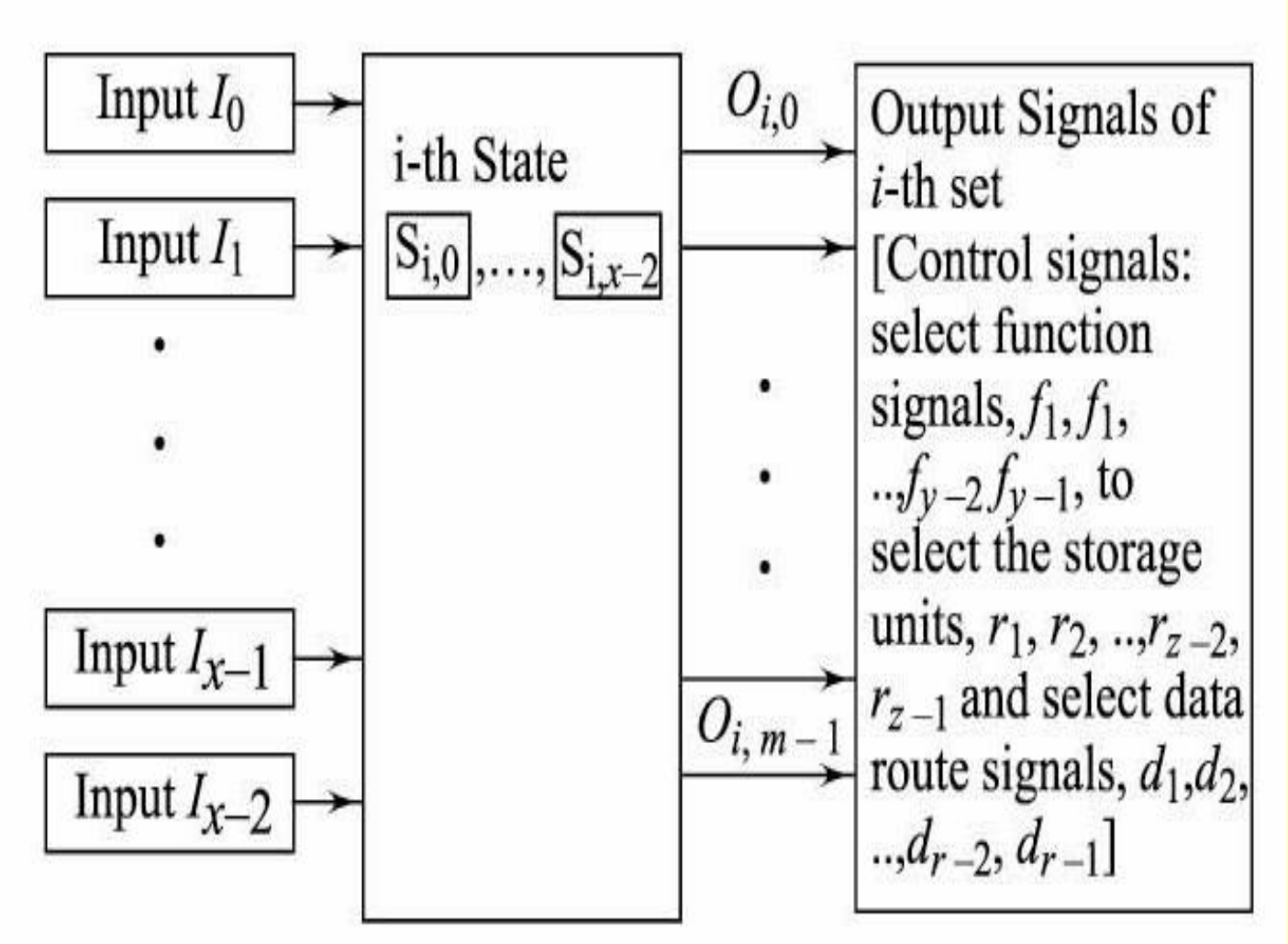
Outputs $O_{i,\,0}$ to $O_{i,\,m-1}$ in sequentially generated states

Hardwired Control Unit Outputs $O_{i,0}$ to $O_{i,m-1}$ in sequentially generated states

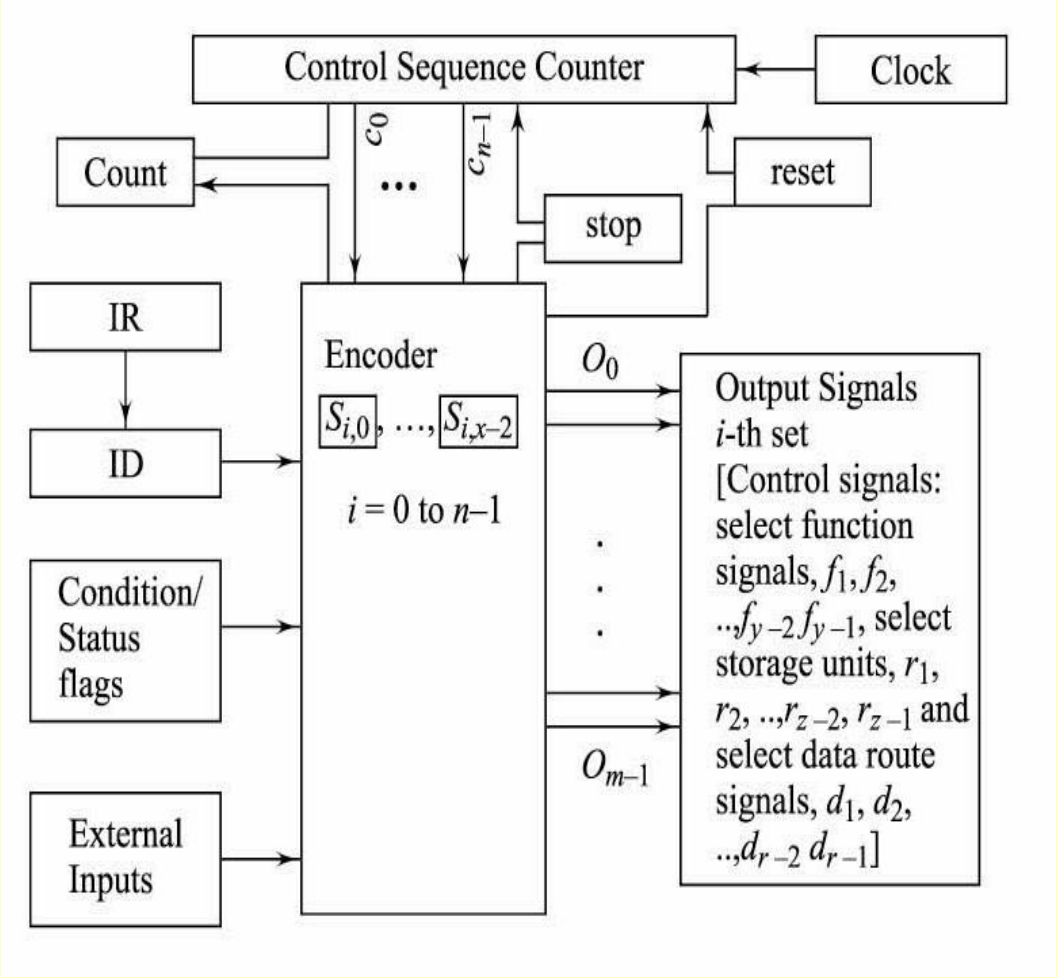
- The outputs $O_{i,0}$ to $O_{i,m-1}$ in case of each state—3 types of control signals

1. Select function signals, $f_1, f_2, .., f_{y-2}, f_{y-1}$
2. Select storage units, $r_1, r_2, .., r_{z-2}, r_{z-1}$
3. Select data route signals, $d_1, d_2, .., d_{r-2}, d_{r-1}$

Moore state machine i^{th} set of outputs for given set of inputs in the i^{th} state



Hardwired control unit organization using a sequence counter from 0 to $n-1$



Encoder to generate states with outputs $O_{i,\,0}$ to $O_{i,\,m-1}$ in sequentially generated states

Hardwired Control Unit Organization

- An encoder takes input from a sequence counter, instruction decoder, condition/status flags and external inputs
- External inputs can be from an external interrupting source and an external device requesting access to external buses
- Condition/status flags are as per conditions/ status flags set in earlier instructions

Control Unit Organization

- The encoder sends a reset signal after the end of an instruction and a stop signal to the sequencer after the last sequence
- The encoder also sends count start signal to let the clock increment the counter during processing of an instruction
- Three sets of control signals that are outputs in various states

Operations by the control unit

Control Unit Outputs

(1) select function signals, f_1, f_2, ..,f_{y-2}, f_{y-1}

(2) select storage units, r_1, r_2, ..,r_{z-2}, r_{z-1}

(3) select data route signals, d_1, d_2, ..,d_{r-2}, d_{r-1}

Operations by the control unit using encoder output control signals in First two steps

(i) *Step j:* PC →MAR.

(ii) *Step j + 1:* PC ← PC + 4 for 32-bits memory word alignments

The sequence counter

- Resets when an instruction transfers to ID after decoding and starts on encoder activating count signal
- Let c_0, c_1, ..c_{n-1} be the sequence counter output from the instance activation of the count output of encoder

*r*1 to *r*12 storing unit control signals

r1. Storing unit PC output control
r2. Storing unit PC input control
r3. Storing unit MAR output control
r4. Storing unit MAR input control
r5. Constant 4 storing unit output control
r6. Constant 4 storing unit input control

*r*1 to *r*12 storing unit control signals

r7. Input for arithmetic unit *X* output control

r8. Input for arithmetic unit *X* input control

r9. Input for arithmetic unit *Y* output control

r10. Input for arithmetic unit *Y* input control

r11. Arithmetic unit output *Z* input control

r12. *Z* output control

*f*1 to *f*2 function select control signals

f1. Data transfer

f2. Add

*d*1 to *d*4 the data route select control signals

d1. Data route internal bus control

d2. Data route external address bus output control

d3. Data route external data bus output control

d4. Data route external data bus input control

- *Step j:* PC → MAR implements by a control signal *r*4 ← c0.*f*1.*d*1.*r*1.
- *Step j* + 1: PC → PC + 4 implements in the next sequence by a control signal *r*2 ← *c*1.*f*1.*d*1.*r*6.*r*5.*r*8.*r*7.*r*1. *r*10.*r*9.*f*2.*r*11.*r*12.

Control Unit—Hardwired Control

- When all the encoder output control signals at each step and sequence generates by hardware, the encoder hardware implements from the start of count to the end stop state
- When the encoder circuit outputs control signals for each input from instruction decoder register ID, the control unit is said to be hardwired control

States

- Let i-th state *Si* be represented by those signals among the select function signals, f_1, f_2, ..,f_{y-2}, f_{y-1}, select storage units, r_1, r_2, ..,r_{z-2}, r_{z-1}, and select data route signals, d_1, d_2, ..,d_{r-2}, d_{r-1} that are active at the i-th sequence
- Each control signal output set *Ci* from encoder

Output set *Ci*

- $Ci = c0.S0 + c1.S1 + \ldots\ldots$ for a given set of inputs from ID, flags, and external inputs. [The plus sign means an OR operation and dot means an AND operation]
- Each control signal activates or does not activate as per instruction given at the ID during a given set of steps (sequence)

Summary

We learnt

- Design of hardwired control unit to generate all sequences of the control signals
- An encoder for the outputs of control signals at each step and generates sequence by hardware from the start of count 0 to the end state
- Encoder circuit outputs the control signals for given inputs from ID, status flags and sequence counter in the hardwired control

We learnt

- Control signals to select function, f_1, f_2, ..,f_{y-2}, f_{y-1}
- Select storage units, r_1, r_2, ..,r_{z-2}, r_{z-1}
- Select data route signals, d_1, d_2, ..,d_{r-2}, d_{r-1}

End of Lesson 13

Hardwired control