Lesson 11:

Multiple Bus Organisation

Objective

- Understand multiple bus organisation

- Learn how the number of independent steps can be clubbed into single step in a multiple bus organization

- Learn how a Processor performance improves by a multiple bus organization

Single bus

Single bus

- Permits a number of units to be connected together through a common set of wires

- Bus connections─ such that the normal state of each subunit (when not active) is tristate

- Each subunit activates and takes input from the bus or sends an output to the bus when a tristate input or output gate activates

Single bus

- The tristate input-gate activate by a control signal ϕ_i and output can be activated by another control signal θ_j

- Tristate— inactive state or high impedance state

Example of 4 tristate units on a common bus and two set of gates
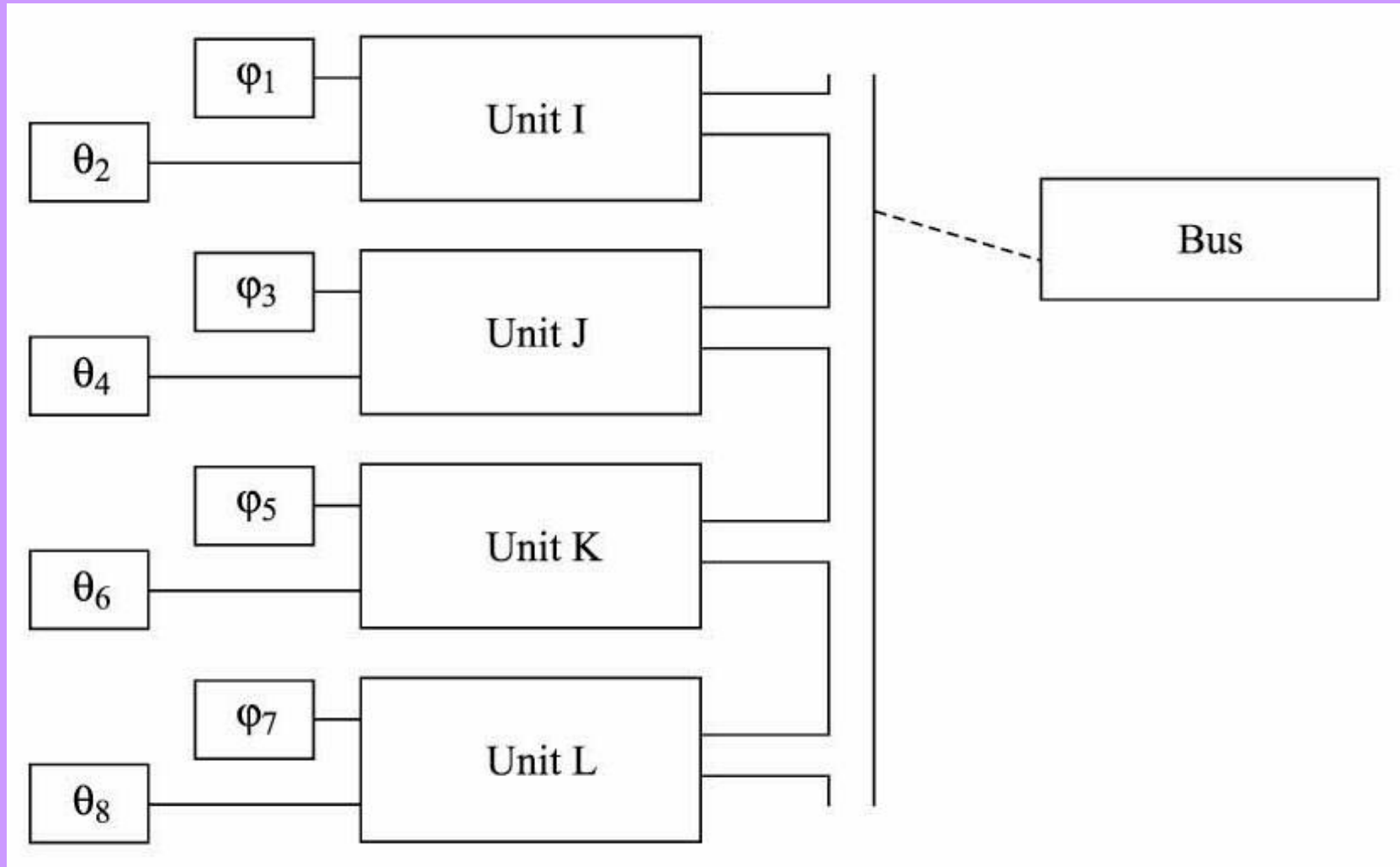
unit J → unit I

- Assume ─ a control unit simultaneously activates ϕ_1 and θ_4
- Unit J gates activates and connects the bus to send the output to the bus
- Unit I gates activates and connects the bus to get the input from the bus
- The transfer operation ─ unit J → unit I

unit $K \rightarrow$ unit L

- Assume─ the control unit simultaneously activates ϕ_7 and θ_6
- Unit K gates─ activate and connects the bus to send the output to the bus
- Unit L gates activate and this connects the bus to get the input from the bus
- unit $K \rightarrow$ unit L

Simple processing units' interconnections and simpler processor microarchitecture

- All subunits— registers *ri* and *rj*, PC, MAR, MDR, TEMP, Offset, *X*, *Y*, Z, IR, ID, MUX, and others — connect a bus

- Using the same bus, a control unit issues control signals to the input and output tristate gates and the processor takes steps *i*, or *j*, or *k*, for arithmetic operations, fetching an instruction or data, storing a word in memory, and branching, respectively

Two buses
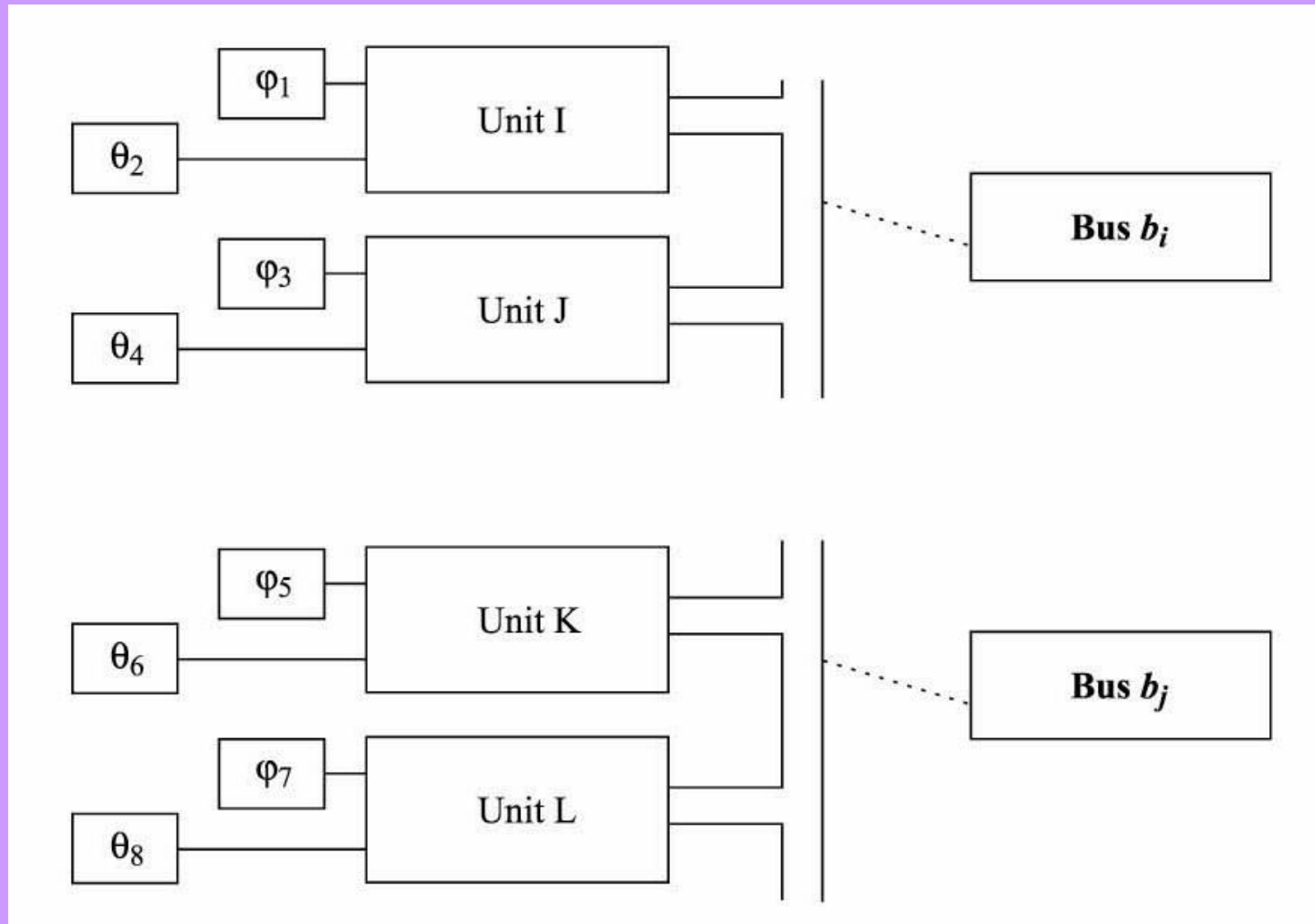
Four units with two control-gates each

- One control gate for enabling input connections from the bus

- Second to enable output connections to one of the buses

- The tristate input gates can be activated by a control signal ϕ_i, and at output can be activated by another control signal θ_j at each of the bus

- $i = 1, 3, 5$ or 7

- $j = 2, 4, 6$ or 8

unit $J \rightarrow$ unit I and unit $K \rightarrow$ unit L

- Assume processor control unit simultaneously activates ϕ_1, θ_4, ϕ_7, and θ_6

- Two set of transfer operations— simultaneously unit $J \rightarrow$ unit I and unit $K \rightarrow$ unit L

Two buses

- Help in performing two sets of independent steps simultaneously with the help of a control unit

Processor performance improvement by a multiple bus organization

- While the steps still have to be performed by sequentially changing from one step to another, the number of independent steps can be clubbed into single step in a multiple bus organization

Simultaneous Operations

- The operations i (MUX $\rightarrow$ X) and $i + 2$ (Input operand $\rightarrow$ Y) independent and simultaneously if there are two buses

- The operations $i + 1$ (X $\rightarrow$ ALU) and $i + 3$ (Y $\rightarrow$ ALU) are independent and could have been done simultaneously if there are two buses

- Four steps would have been reduced to two steps, i' and $i' + 1$

Summary

We Learnt

- Multiple bus organisation
- Clubbing of number of independent steps into single step in a multiple bus organization
- Improvement in performance in a multiple bus organization

End of Lesson 11 on
Multiple Bus Organisation