Chapter 05: Basic Processing Units … Control Unit Design Organization

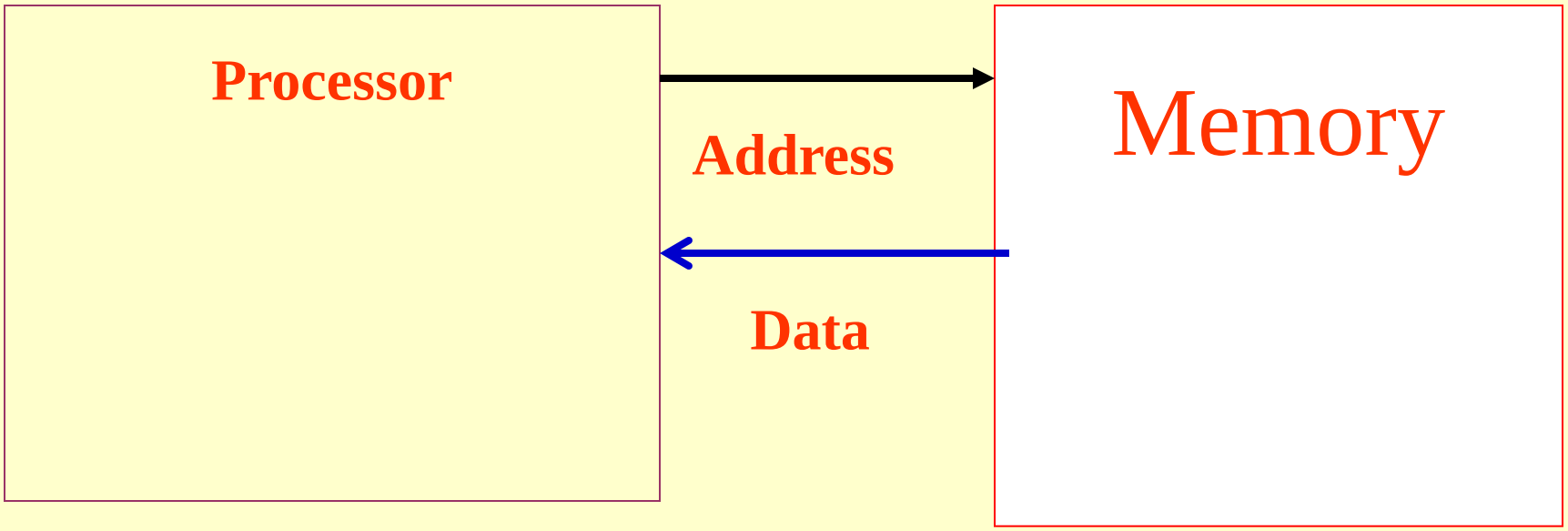
Lesson 10:
Execution of a branch instruction

Objective

- Learn microoperations for a branch instruction

Steps for branch instruction operations

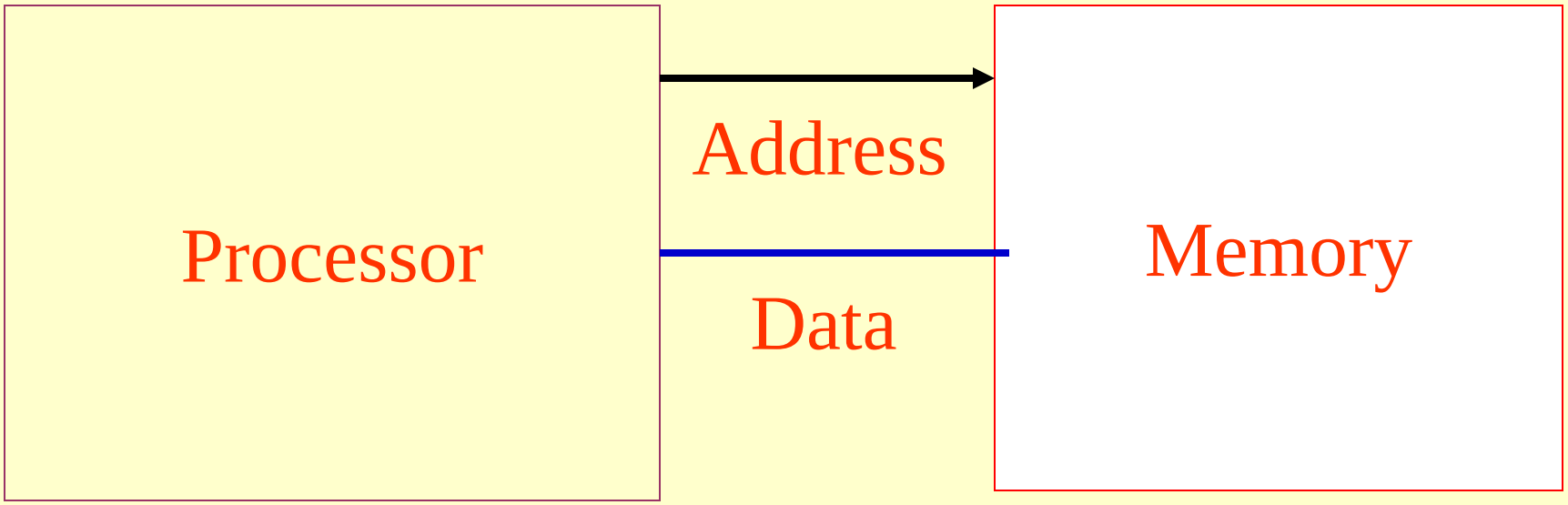
Instruction Fetch



Step 1) Processor requests instruction from memory using address in Program Counter PC register

Step 2) Memory using data bus returns the instruction to instruction register IR register

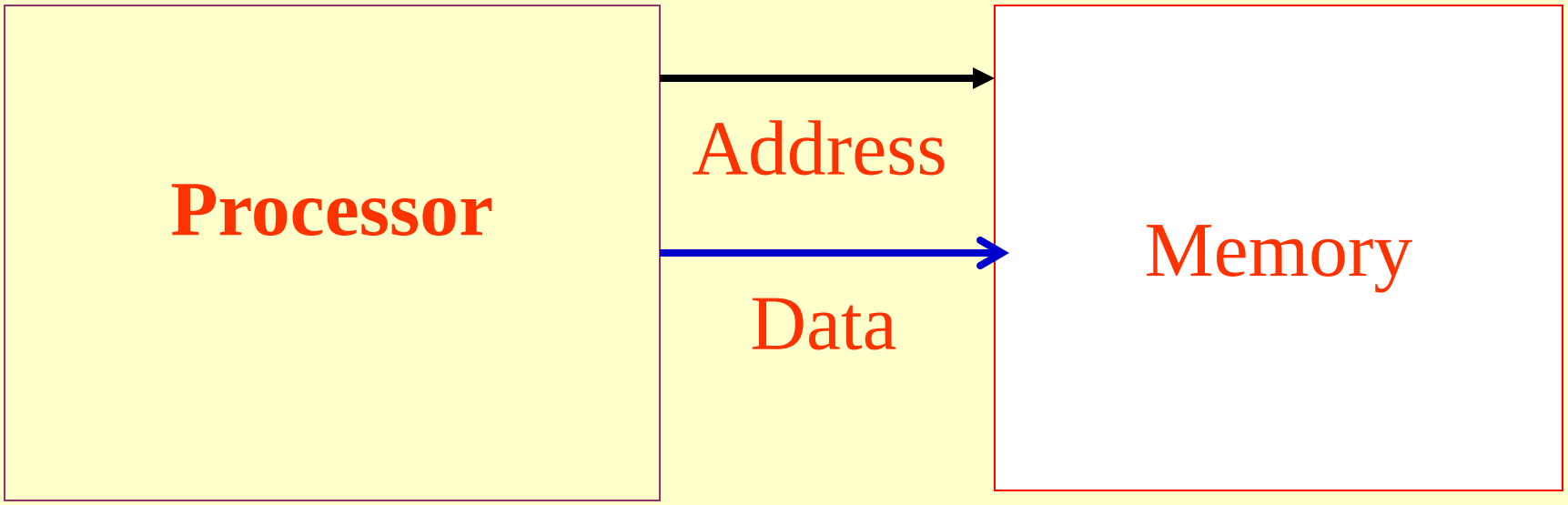
Instruction decoding and execution



Step 3) Processor decodes instruction and places at instruction decoder ID register

Step 4) Processor executes instruction at execution unit by finding the branch address value by operands

Result Write back and PC update for the next



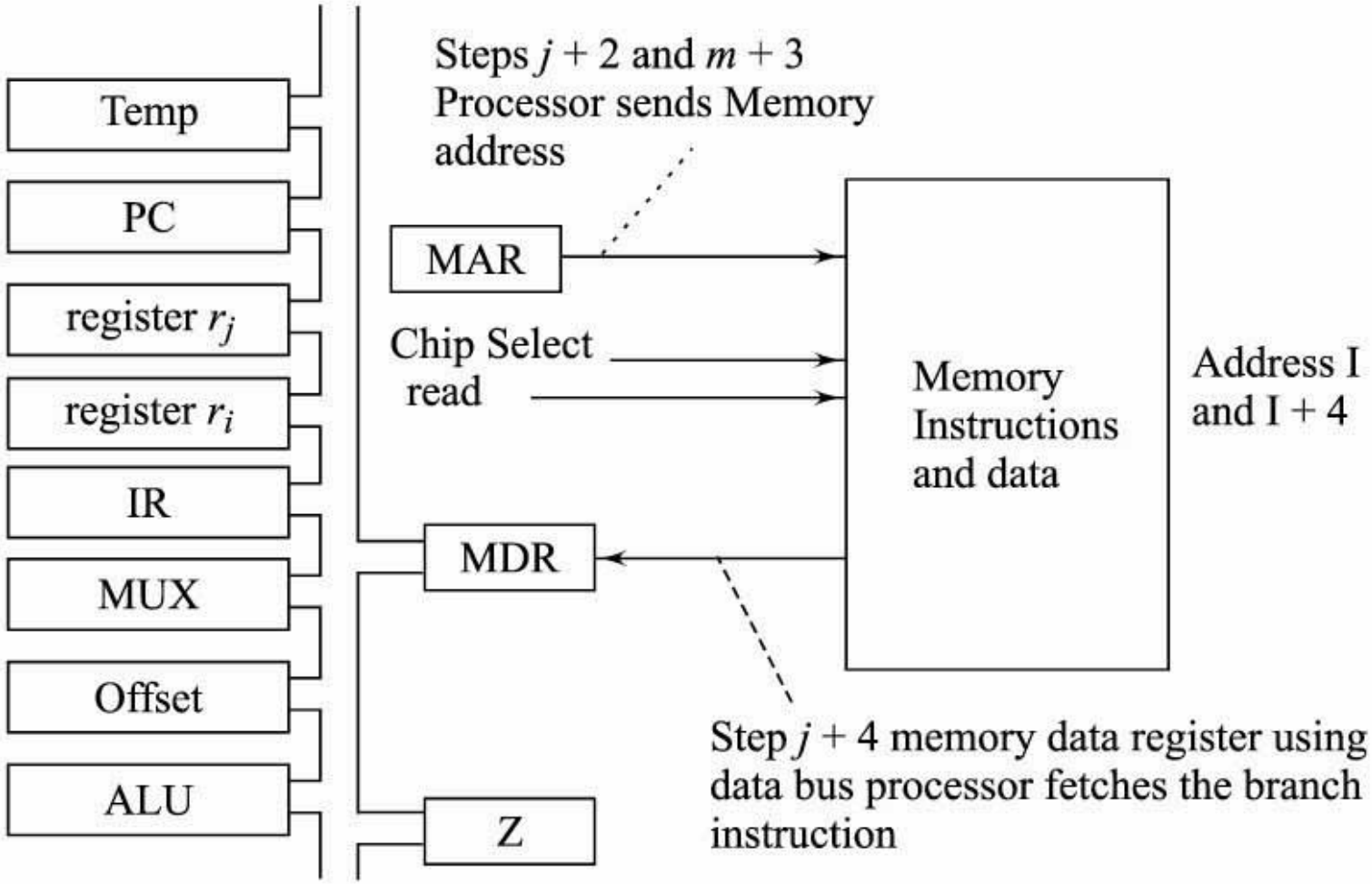
Step 5) Result of instruction written back for PC

Step 6) PC transfers to MAR for next instruction

Execution of a Complete Instruction by Data Path Implementation

- Execution of a branch instruction can be considered as the implementation of a specific data path flow, as per the specific instruction
- The processing unit composition is as controlled data-path unit and control unit (controlling and sequencing unit)
- Control unit generates control signals to implement each step using signals ϕs to enable new branch address into PC and then in MAR

Processing subunits during branch instruction



Microoperations during branch instruction fetch

1. *Step j*: PC transfers MAR through internal bus
   PC → MAR
2. *Step j* + 1: For instruction last byte fetch case,
   PC → PC + 4 for 32-bits memory word alignment

Microoperations during branch instruction fetch

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7. Step $j + 6$: MDR transfers through internal bus MDR $\rightarrow$ IR, GPR, or another word-storing unit through bus or a MUX.
8. Repeat steps $j + 2$ to $j + 6$ if instruction opcode and operands fetch is not complete

Microoperations during branch instruction after fetch of opcode and operands

- Assume that IR gets a BR *absolute address* instruction
- Then, then step *l* following steps will be implemented, after Step *j* to *j* +6, to fetch the instruction opcode and operands else step *m*
- Step *l*: Operand address with the instruction absolute address → PC

Microoperations during conditional branching with an operand as offset

1. *Step m:* Test comparison condition
2. *Step m + 1:* If comparison condition found the offset then it adds into PC

- The operation PC + offset → Temp

3. *Step m + 2:* Temp → PC
4. *Step m + 3:* PC → MAR

Summary

We Learnt

- Instruction steps in completing all microoperations during branch
- Fetch instruction
- Read operands
- Execute instruction operand transfer to PC in case of branch absolute
- Execute instruction operand transfer to PC in case of branch condition satisfied

End of Lesson 10 on

Execution of a branch instruction