Chapter 05: Basic Processing Units … Control Unit Design Organization

Lesson 05:

Instruction fetch in a data path implementation

Objective

- Learn a how instruction fetches from a memory address

Transfer to Instruction Register

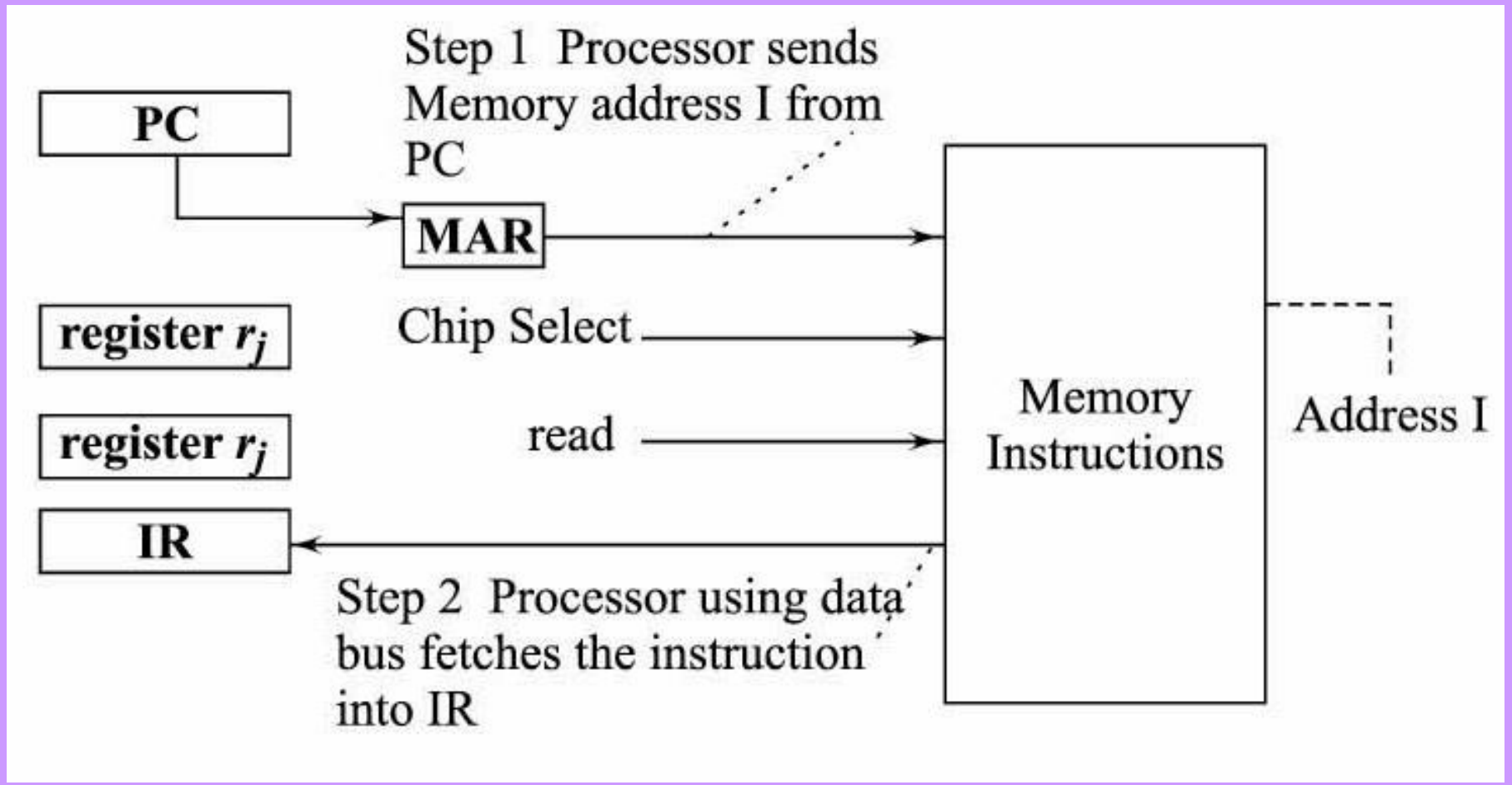
Execution of an Instruction by Data Path Implementation

- Execution of an instruction can be considered as the implementation of a specific data path flow, as per the specific instruction
- The processing unit composition is as controlled data-path unit and control unit (controlling and sequencing unit)
- Control unit generates control signals to implement each step using signals ϕs

Step before execution of an instruction

- Fetch the instruction – directly from memory or through a cache
- An instruction fetch using memory address register (MAR) and the content of the instructions in memory transfer to instruction register (IR)

Instruction fetch into instruction register IR



Representation of microoperation during instruction fetch

- Assume instruction at a memory address M[**I**], where **I** is the address of the instruction **I**
- Step 1 in Fetch process–

MAR ← PC

Address_Bus ← MAR

- Step 2 in Fetch process–

RD: Data_Bus ← M[I]

IR ← Data_Bus

Program Counter Register Increment before initiating fetch of instruction

A sequence of program counter register (PC) during four instruction cycles at the processor

- A step before fetch of an instruction─ transfer the PC after required increment to fetch the instruction– directly from memory or through a cache

Sequences of microoperations in fetch process for a new cycle

- Assume that memory stores *m* byte words at addresses in multiple of 4
- Sequences of microoperations in fetch process for a new cycle after the program counter increment

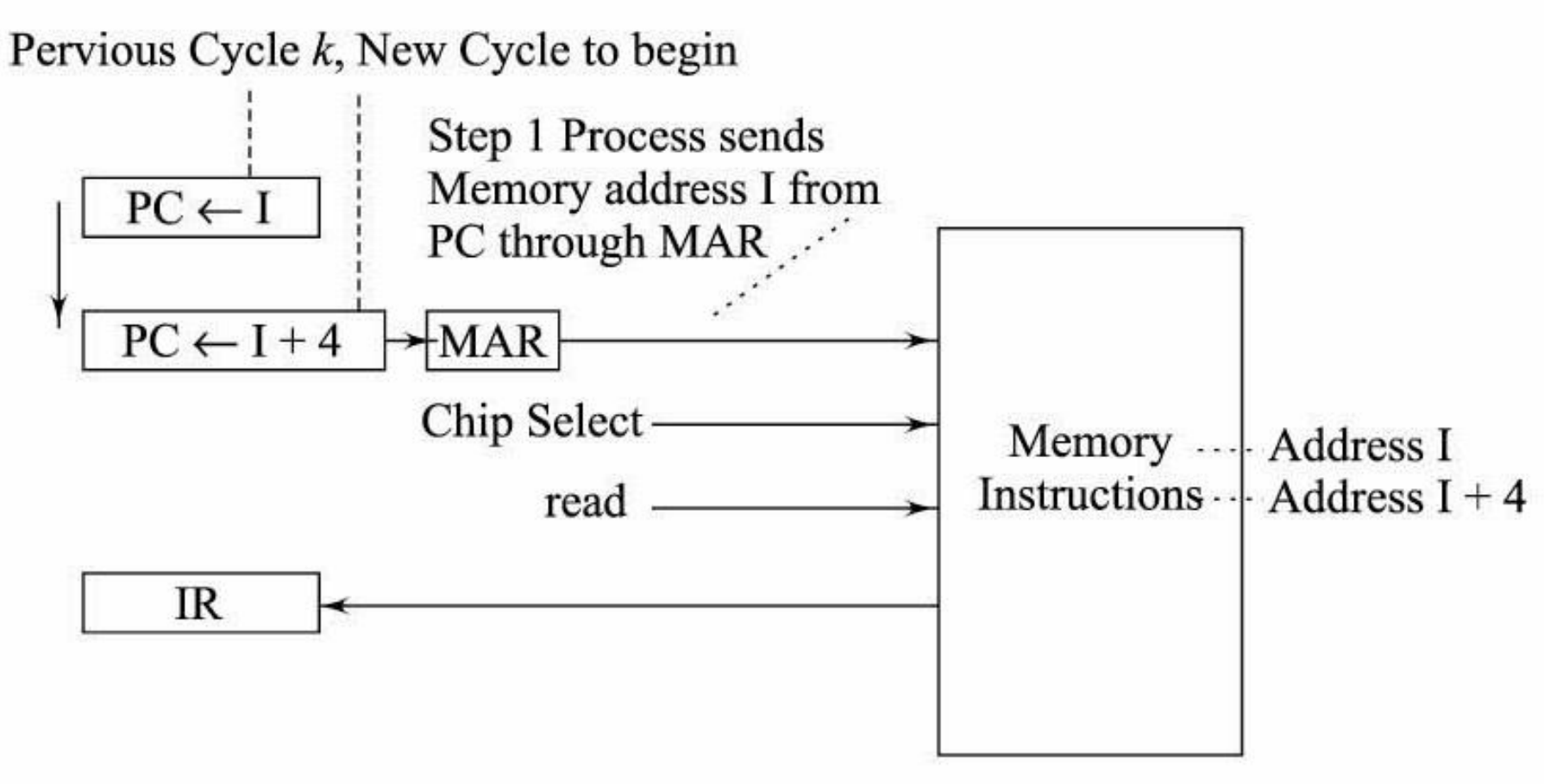
Steps

- Step 0: I = I + m and I → PC
- Step 1: MAR → PC and PC → Address_Bus
- Step 2: Data_Bus ← M[I] and IR ← Data_Bus

Memory storing 4 byte words at addresses in multiple of 4

- Sequences of microoperations in fetch process for a new cycle
- Step 0: I = I + 4 and I → PC
- Step 1: MAR → PC and PC → Address_Bus
- Step 2: Data_Bus ← M[I] and IR ← Data_Bus

Increment of PC always happening before a fetch process of next instruction and after the previous fetch



Summary

We Learnt

• Register transfer into IR from the memory address of instruction
• Program counter defines address to fetch a word from memory through the address register MAR and address bus signals
• Increment of PC always happening before a fetch process of next instruction and after the previous fetch

End of Lesson 05 on

Instruction fetch in a data path implementation