Chapter 05: Basic Processing Units … Control Unit Design Organization

Lesson 04

Bus, register and Memory transfer for data path implementation

Objective

- Understand transfer between Processor registers through buses
- Understand transfer between Processor register and memory through buses
- Understand data path implementation

Bus Transfer from or to processor register

- Multiple registers can be connected to a common bus using a multiplexer
- Multiplexer– a logic unit which takes multiple source inputs but sends only one source input in the output as per the source select control inputs

Control signals

- Input control input during interval T─ IN
- Register select Control inputs during interval T ─ RS2 RS1 RS0

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 000
- Action on 1000 Bus $\rightarrow$ r0

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 101
- Action on 1101 Bus $\rightarrow$ r5

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 001
- Action on 1001 Bus $\rightarrow$ r1

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 010
- Action on 1010 Bus $\rightarrow$ r2

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 011
- Action on 1011 Bus $\rightarrow$ r3

Control signals: INRS2RS1RS0 and action on the data path

- IN = 1
- RS2RS1RS0 = 100
- Action on 1100 Bus $\rightarrow$ r4

Control signals

- Output control output during interval T'─ Out
- Register select Control outputs during interval T' ─ RS2 RS1 RS0

Control signals: outRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 000
- Action on 1000 Bus ← r0

Control signals: OUTRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 001
- Action on 1001 Bus ← r1

Control signals: OUTRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 111
- Action on 1111 Bus ← r7

Control signals: OUTRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 010
- Action on 1010 Bus ← r2

Control signals: OUTRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 111
- Action on 1011 Bus ← r3

Control signals: OUTRS2RS1RS0 and action on the data path

- OUT = 1
- RS2RS1RS0 = 110
- Action on 1110 Bus ← r6

Microoperation r5 ← r1 using datapath by two sequences of Control signals

- A sequence of control output at T ─ INOUTRS2RS1RS0
- A sequence control output at T' ─ INOUTRS2RS1RS0
- At T─ control sequence INOUTRS2RS1RS0 = 01001 : Bus ← r1
- At T' ─ control sequence INOUTRS2RS1RS0 = 10101: Bus → r5

Microoperation r1 ← r3 in datapath by two sequences of Control signals

- At T ─ control signals' sequence INOUTRS2RS1RS0 = 01011: Bus ← r3
- At T' ─ control signals' sequence INOUTRS2RS1RS0 = 10101: Bus → r5

Memory Read

Memory transfer microoperation through the bus to processor register MDR

- Active during an interval T when the corresponding address select control bits are active and memory read control output RD to memory enables (=1)
- Implements the transfer along the data path by microoperation from memory address to MDR

Memory read Microoperation in three control sequences T, T' and T"

- ADDR: A31-A0, and RD and WR in tristate at T
- RD: Bus ←M(Addr) and WR in tristate at T'
- RD: MDR ← Bus and WR in tristate at T"

Memory write

Memory transfer microoperation through the bus from processor register MDR

- Active during an interval T when the corresponding address select control bits are active and memory write control output WR to memory enables (=1)
- Implements the transfer along the data path by microoperation from MDR to memory address

Memory write Microoperation in three control sequences T, T' and T"

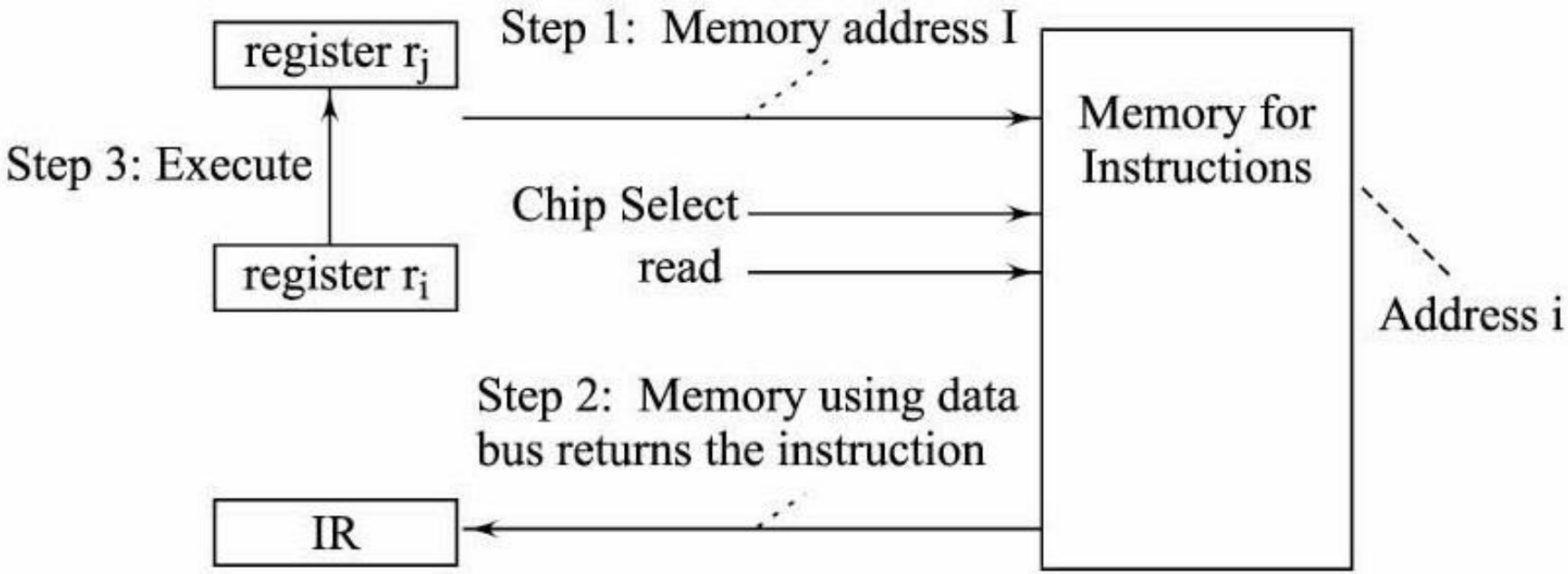
- ADDR: A31-A0, and RD and WR in tristate at T
- WR: MDR → Bus and RD in tristate at T'
- WR: Bus → M(Addr) and RD in tristate at T"

Memory transfer microoperation through the bus from processor register MDR

- Active during an interval T' when the corresponding address select control bits are active and memory write control output WR to memory enables (=1)
- Implements the transfer along the data path by microoperation from MDR to memory address

Data path implementation

MOV rj, ri in Step 3



Implementation of path for register transfer by 3 sets of control signal sequences

- Set of Control Sequences 1: Implementation of path for reading instruction from a memory address to Instruction Register
- Set of Control Sequences 2: Control Sequences 2: Implementation of path for register transfer from IR to Instruction decoder
- Set of Control Sequences 3: Implementation of path for register transfer from ri to rj

Summary

We Learnt

- Bus transfer by control signals IN and OUT or RD and WR
- Register selection by RS2RS1RS0
- Memory address selection by A31:A0

End of Lesson 04 on

Bus, register and Memory transfer for data path implementation