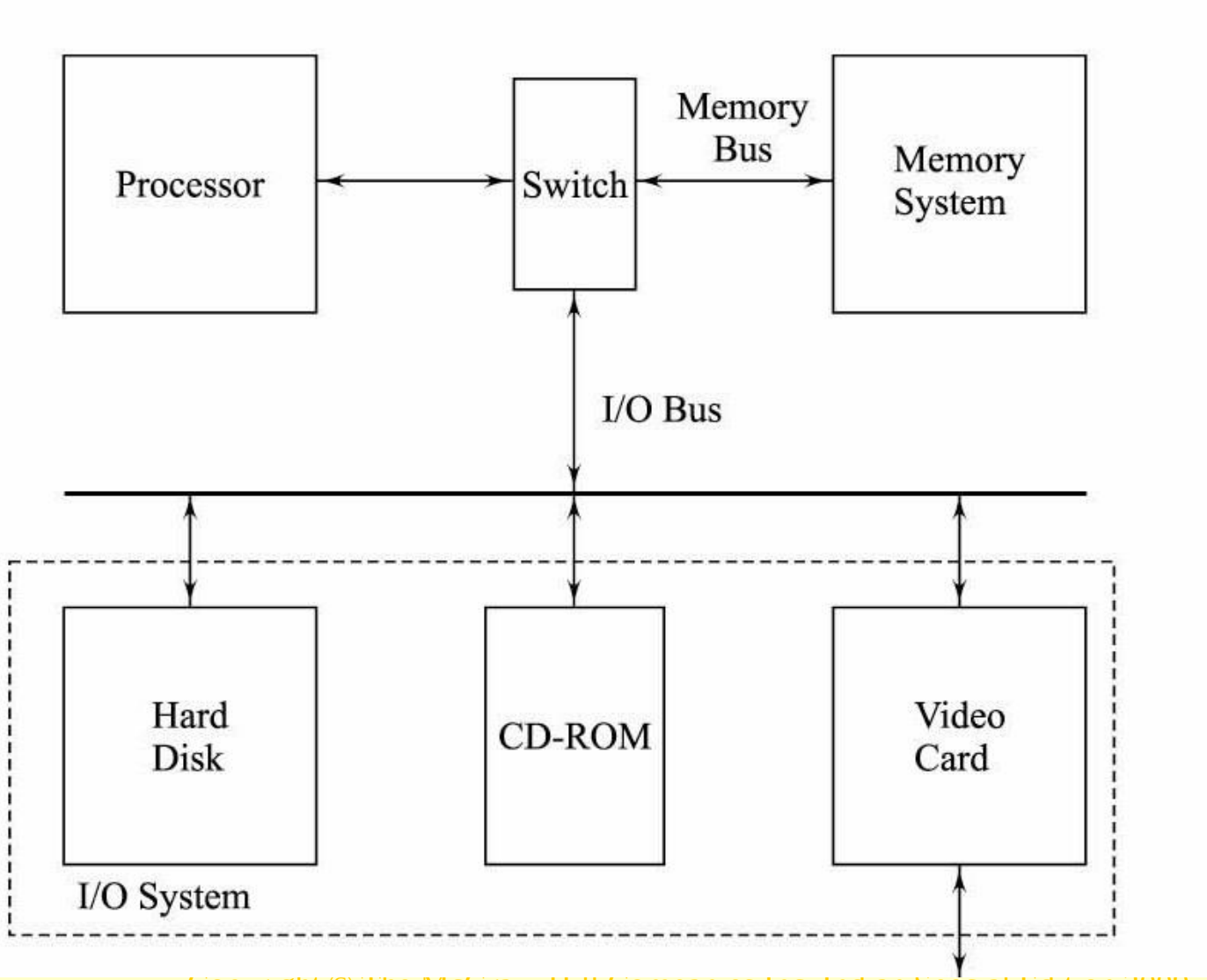
Chapter 05: Basic Processing Units … Control Unit Design Organization

Lesson 02:

Bus Architecture

Memory Bus (System Bus)

Bus Interconnection of Processor units to memory and IO subsystem



Memory bus

- Memory bus (also called system bus since it interconnects the subsystems)
- Interconnects the processor with the memory systems and also connects the I/O bus.
- Three sets of signals –address bus, data bus, and control bus

System Bus

- A system's bus characteristics — according to the needs of the processor, speed, and word length for instructions and data.
- Processor internal bus(es) characteristics differ from the system external bus(es).

Address, Data and Control Buses

Address Bus

- Processor issues the address of the instruction byte or word to the memory system through the address bus
- Processor execution unit, when required, issues the address of the data (byte or word) to the memory system through the address bus

32-bits Address Bus

- The address bus of 32-bits fetches the instruction or data from an address specified by a 32-bit number

Address Bus Example

- Let a processor at the start reset the program counter at address 0
- Then the processor issues address 0 on the bus and the instruction at address 0 is fetched from memory

Address Bus Example

- Let a processor instruction be such that it needs to load register r1 from the memory address M
- The processor issues address M on the address bus and data at address M is fetched

Data Bus

- When the Processor issues the address of the instruction, it gets back the instruction through the data bus
- When it issues the address of the data, it loads the data through the data bus
- When it issues the address of the data, it stores the data in the memory through the data bus

32-bit Data Bus

- A data bus of 32-bits fetches, loads, or stores the instruction or data of 32-bits

Data bus use example 1

- When the processor issues address *m* for an instruction, it fetches the instruction through data bus from address *m*
- For a 32-bit instruction, the word at data bus is fetched from addresses m, m + 1, m + 2, and m + 3

Data bus use example 2

- When an instruction is given to store register r1 to the memory address M, the processor issues address M on the bus and sends the data at address M through the data bus
- For 32-bit data, word at data bus is to the memory addresses M, M + 1, M + 2, and M + 3

Control Bus

- Issues signals to control the timing of various actions during interconnection
- Bus signals synchronize the subsystems

Control Bus Signals

- Control signals as per the processor design

Control Bus Signals

- Control bus issues signals to control the timing of various actions during interconnection
- Control bus signals from processor to Memory read, Memory write, IO read, IO write
- Control bus signals synchronize the subsystems: memory and IO systems
- Control bus signals from processor to Address latch enable or data valid

Control Bus Signals

- Control bus signals from systems to processor for Interrupt and hold
- Control bus signals from processor to systems for Interrupt acknowledge, hold acknowledge

Control bus uses example 1

- When the processor issues the address, it also issues a *memory-read* control signal and waits for the data or instruction
- Memory unit must place the instruction or data during the interval in which memory-read signal is active (not inactivated by the processor)

Control bus uses example 2

- Let the processor issues the address on the address bus, and (after allowing sufficient time for the all address bits setup) it places the data on the data bus

CONTROL BUS USE EXAMPLE 2

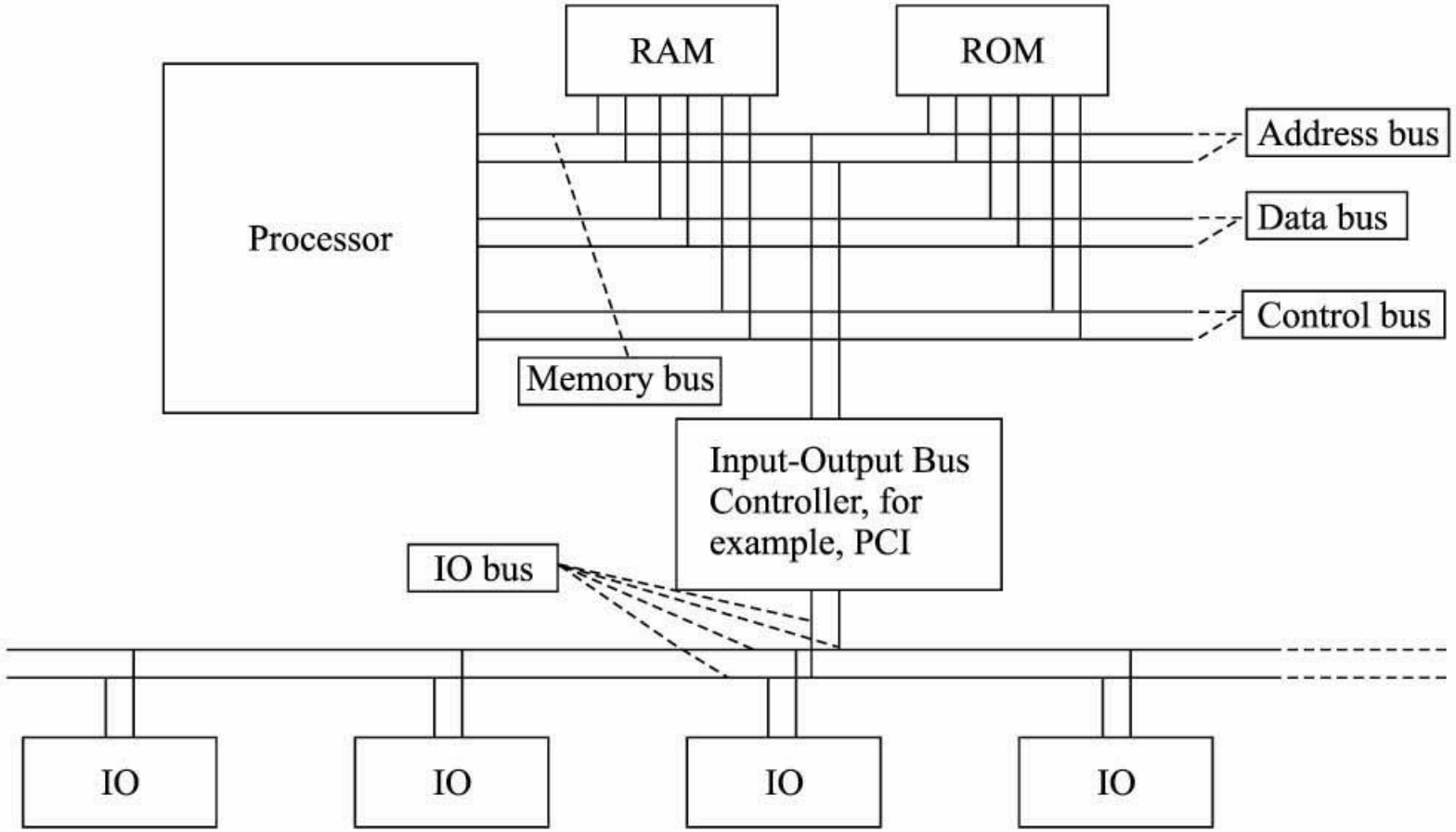
- Also then issues *memory-write* control signal (after allowing sufficient time for the all data bits setup) for store signal to memory. The memory unit must write (store) the data during the interval in which memory-write signal is active (not inactivated by the processor).

IO Bus and PCI Bus

Devices on I/O Bus

- Devices can be designed to interface with the bus, allowing them to be compatible with any computer that uses the same type of I/O bus

Buses to interconnect the processor Functional units to memory and IO subsystem



Summary

We learnt

- Data bus from and to processor
- Address bus from processor to address memory and I/O systems
- Control bus issues signals to control the timing of various actions during interconnection
- Control bus signals from processor to Memory read, Memory write, IO read, IO write

We learnt

- Control bus signals synchronize the subsystems
- Control bus signals from processor to Address latch enable or data valid and from systems to processor for Interrupt and hold
- Control bus signals from processor to Interrupt acknowledge, hold acknowledge

End of Lesson 02 on

Bus Architecture