Chapter 04: Instruction Sets and the Processor organizations

Lesson 19:
CISC Architectures

Objective

- Learn the CISC Architecture

Complex instruction set and variable length instructions

Complex Instruction Set Computer (CISC)

- Has a complex instruction set
- Variable length encoding of instructions
- Instruction execution takes a varying number of clock cycles

Complex Instruction Set Computer (CISC)

- Large number of addressing modes for the operations and instructions, the CISC computer generally requires fewer instructions than-RISC computers to perform the computation
- In addition, programs writing for CISC architectures tend to take less space in memory

Many addressing modes in the instructions

Complex Instruction Set Computer (CISC)

- Arithmetic and other instructions may read the inputs from or write their outputs to the memory system, in addition to use of GPRs register file by arithmetic and other instructions

Hardware required to implement the CISC processor

- More complex, since it would have to be able to fetch instruction operands from memory, so the CISC processor would probably have a longer cycle time (or would require more cycles to execute each instruction) than the RISC processor

Complex Instruction Set Computer (CISC)

- One instruction in a CISC architecture for ADD (rl), (r2), (r3) without load-store architecture
- Load-store architecture means that arithmetic and logic instructions do not use operand at the memory but operands must first load in the registers

Complex Instruction Set Computer (CISC)

- A CISC architecture might allow an ADD operation of the form ADD (rl), (r2), (r3)
- Parentheses around a register name indicates that the register contains the address in memory where the operand can be found or the result should be placed

Load-store architecture to implement CISC ADD (rl), (r2), (r3) operation

- Assume— that the appropriate memory addresses are present in r1, r2, and r3 at the start of the instruction sequence
- Four instructions are required to implement the same function

Four required instructions

- LD r4, (r2)
- LD r5, (r3)
- ADD r6, r4, r5
- ST (r1), r6

Summary

We learnt

- CISC variable length instructions in multiple cycles
- Large number of instructions in the instruction set as number of addressing modes are permitted for operations
- CISC require fewer instructions from memory

End of Lesson 19 on

CISC Architecture