Chapter 04: Instruction Sets and the Processor organizations

Lesson 07:

Instruction Set Features

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Objective

- To understand Instruction set features in a processor

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Operations by the Instructions

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Operations by the Instructions

(1) Data Transfer Operations: These are the memory transfer operations and register transfer operations

- The instructions are ‘Load and Store Instructions’ and Register Transfer Instructions’

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Operations by the Instructions

(2) Program Flow Control Instructions: These are:

(i) Branching instructions

(ii) Condition Codes and branch on condition Instructions

(iii) Subroutine call and return and interrupt related program flow control instructions

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Operations by the Instructions

(3) Arithmetic and Logic operations related instructions

(4) Input and Output Instructions

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Instruction Set

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A processor instruction set

- Defines all the instructions and an instruction among them only can be used in a program, which runs on the processor
- Has the instructions in pre-defined formats

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Unique Instruction set and instruction format

- The instruction set and instruction formats of the instruction in that set are unique for a processor
- As per the processor design
- As per internal ALU and control circuits

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Processor Instruction Set features

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Processor Instruction Set

(i) Based on one-address, two-address, three address or zero address machine architecture

(ii) May be of CISC or RISC instruction set types or a converged set between CISC and RISC

(iii) May or may not be having regularity, orthogonality, completeness and efficiency

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CISC Processor Instruction Set features

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CISC

- The computer that contains very complex instructions─ Complex Instruction Set Computer (CISC)

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CISC Approach

- Before the 1980s─ a great deal of focus on reducing the "semantic gap" between the languages used to program computers and machine languages

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CISC

- Approach─ Making machine languages more like high-level programming languages would result in better performance by reducing the number of instructions required to implement a program and would make it easier to compile high-level language programs into machine language

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CISC end result of the approach

- Design of instruction sets that contained very complex instructions
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CISC

- Generally require fewer instructions than-RISC computers to perform the computation
- In addition, programs writing for CISC architectures tend to take less space in memory
- The Intel x86 (IA-32) architecture, which uses a CISC instruction set— a dominant PC/workstation architecture in terms number of processors used

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Latest Approach

- After the 1980s─ CISC architectures have dropped complex instructions that were not used sufficiently often to justify their implementation (inclusion in the instruction set)

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RISC Type Instruction Set

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Reducing the instructions

- The simpler instruction sets in the computers
- Easier to compile high-level language programs into machine language using the simpler and reduced instructions in the instruction set

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RISC

- The computer that contains reduced number of instructions in the set— Reduced Instruction Set Computer (RISC)

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Simpler instruction sets

- Often allows them to be implement at higher clock rates than CISC computers
- Allowing them to execute more instructions in the same amount of time

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Simpler instruction sets

- Higher performance─ A RISC processor's increased clock rate allows it to execute its programs in less time than a CISC processor takes to execute its programs (which require fewer instructions)

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Latest Approach

- After the 1990s, RISC architectures have incorporated some of most useful complex instructions from CISC architectures, relying on their micro-architecture to implement these instructions with little impact on the clock cycle

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Regularity, orthogonality, completeness and efficiency

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Regularity of the Set

- Expected instruction opcodes and operands should be available
- For example, if add with carry is available with some addressing modes then subtract with borrow should also be available with same addressing ways from the point of view of regularity

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Regularity of the Set

- If multiplication is available with register operands only then division should also be available with register operands only from the point of view of regularity

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Orthogonality of the Set

- Depending on the architecture, some of the addressing modes may only be available to some of the instructions that reference memory
- Architectures that allow instruction that references memory to use any addressing mode are described as *orthogonal*, because the choice of addressing mode is independent from the choice of instruction

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Orthogonal Set

- Expected pairs of instruction opcodes and operands should be available and with the same set of addressing modes

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Orthogonal Set

- Let add with carry is available with some addressing modes then subtract with borrow as well as other arithmetic and logic operations should also be available from the point of view of orthogonality and with same addressing modes from the point of view of regularity

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Orthogonal Set

- If multiplication is available with register operands and division not available then set is not orthogonal

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Completeness of Set

- Expected instruction opcodes and operands should be available and with the same set of addressing modes
- Completeness may not be explicitly definable
- It should however be possible to do the given computations for a given requirement in reasonable amount of time

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Completeness of Set

- Some times, due to reason of compactness and less often need of an instruction, that instruction may not be provided in an instruction set
- Any computations that are needed most of the times must be available in the set

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Example of Completeness of Set

- For example, multiplication and division may not be provided due to reason of complexity of logic circuits and even some basic instruction may not be provided in a processor instruction set

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Example of Completeness of Set

- 8051 microcontroller has two instructions add and add with carry available but has subtract with borrow only
- Instruction set is incomplete
- Reason─ to make the instruction set compact
- *Subtract* instruction─ can always be implemented using *subtract with borrow* only instruction in two steps── clear carry flag (same as borrow flag) = 0 and execute subtract with borrow

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Efficiency of the Set

- Instruction opcodes and operands most frequently needed should be available for the reason of efficiency
- For example, consider, that MOV r1, r2 can always be implemented by ADD r1, r2 when r1 is first cleared to 0s
- However, the MOV instructions are needed quite frequently in a program
- Therefore, the both MOV and ADD are provided at the instruction sets

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Example of Efficiency in ARM processor

- Instruction set provides for MOV as well as MVN
- The two instructions complement and move are executed together by MVN
- *MOV* ri, rj moves rj bits into ri, meaning (ri) ← (rj). [rj bits do not change]
- *MVN* ri, rj instruction, meaning (ri) ← NOT (rj), move complement of rj bits into ri. (rj bits do not change)

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Example of Efficiency 8051 microcontroller processor

- Instruction set provides for DJNZ R_n, *rel*
- Decrement a register R_n, and jump if R_n is still not zero, else next instruction
- Jump address = next instruction PC + rel and rel is +ve or – ve as it is 8-bit two's complement number
- Implements loop instructions in a program very efficiently

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Compatibility of the Set

- Instruction opcodes and operands should be *compatibility between* different generations of a computer system, meaning that a programmer expects programs that ran on their old system to run on their new system without changes

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Compatibility of the Set

- Instruction set of a new processor is often required to be the same as the instruction set of the company's previous processor
- Sometimes with a few additional instructions
- Most of the design effort for a processor goes into improving the micro-architecture to increase performance

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Summary

We learnt

- Instruction set defines all the instructions
- An instruction among them only can be used in a program, which runs on the processor
- Instruction set has the instructions in pre-defined formats
- CISC, RISC and converged sets in the computers
- Regularity, orthogonality, completeness, efficiency and compatibility of a instruction set

End of Lesson 07 on

Instruction Set Features