

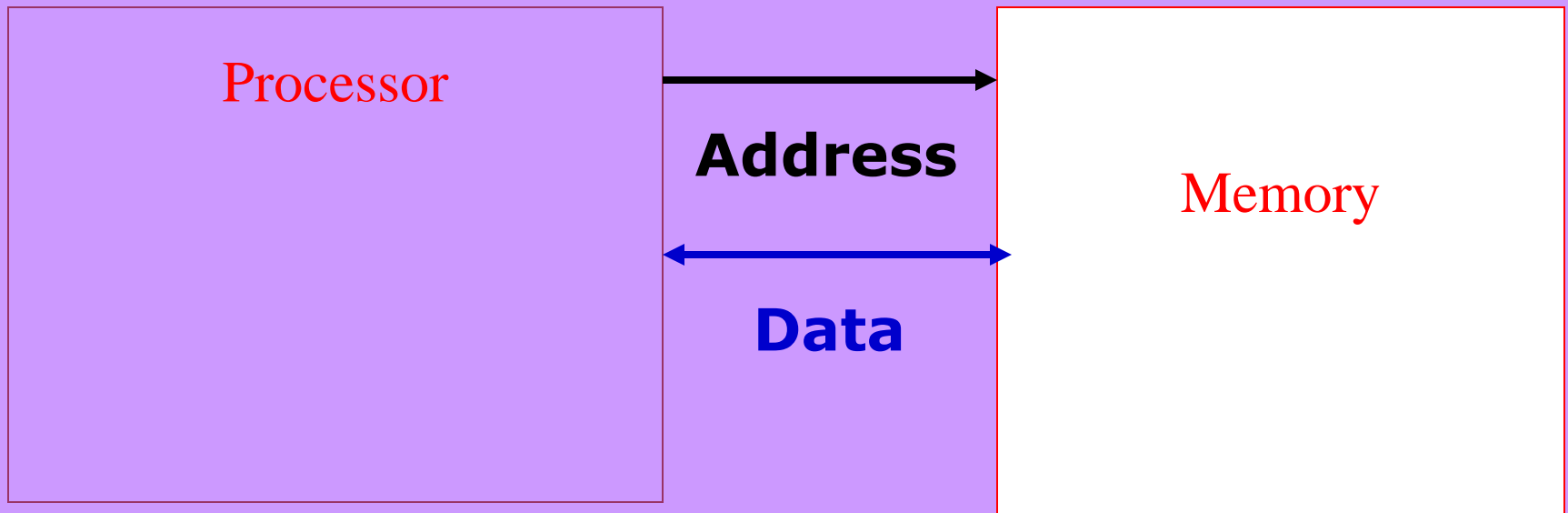
Chapter 04: Instruction Sets and the Processor organizations

Lesson 06: Accessing the operands

Objective

- Understand the operands fetch from memory

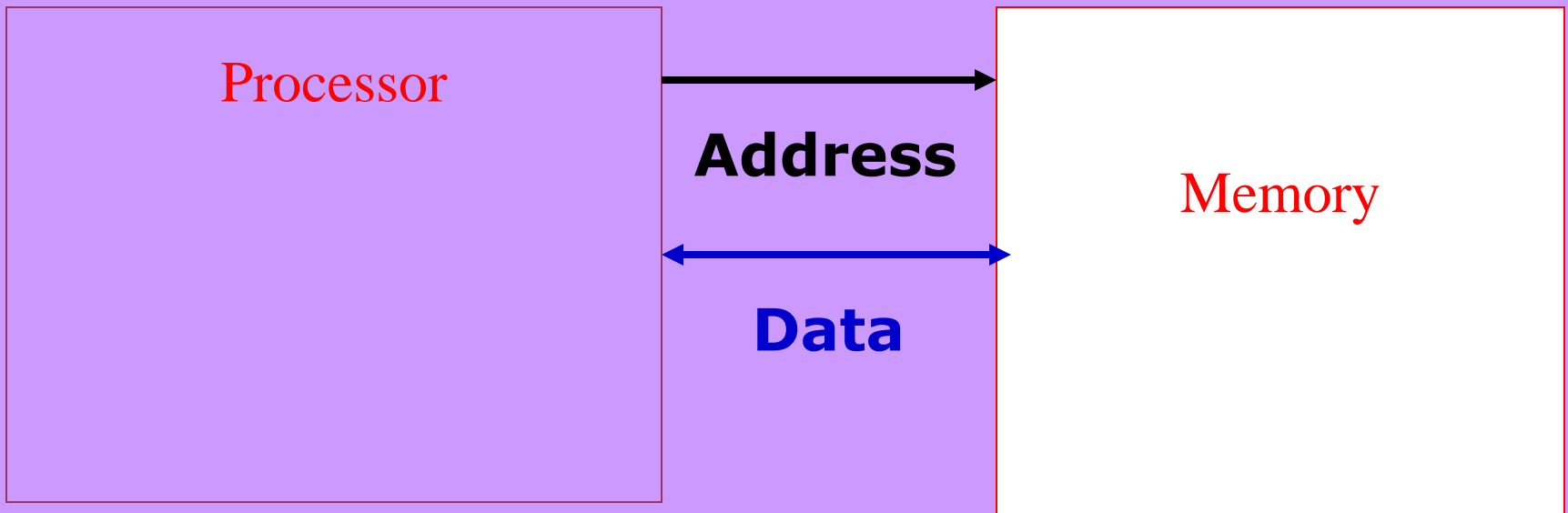
Instruction Fetch



Step 1) Processor requests instruction from memory using address in PC (or IP) register

Step 2) Memory using data bus returns the instruction to IR register

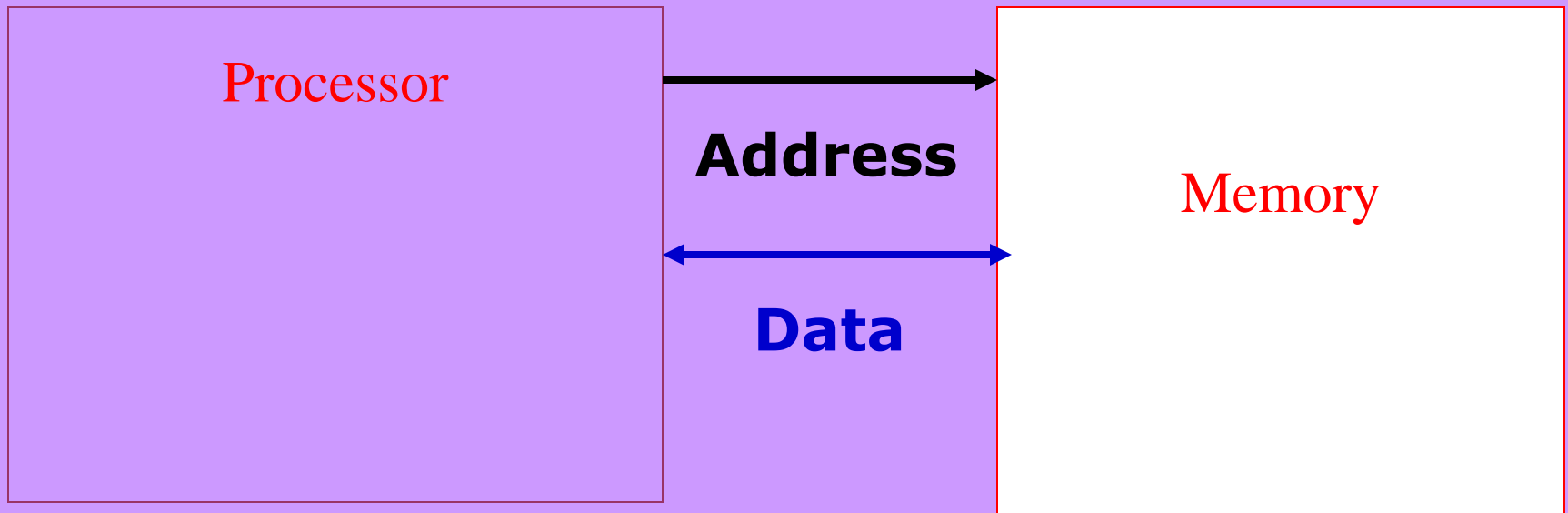
Instruction decoding and execution



Step 3) Processor decodes instruction and places at ID register

Step 4) Processor executes instruction at execution unit

Result Write back and PC update for the next



Step 5) Result of instruction written back for register or memory

Step 6) PC updates for next instruction

Accessing a word

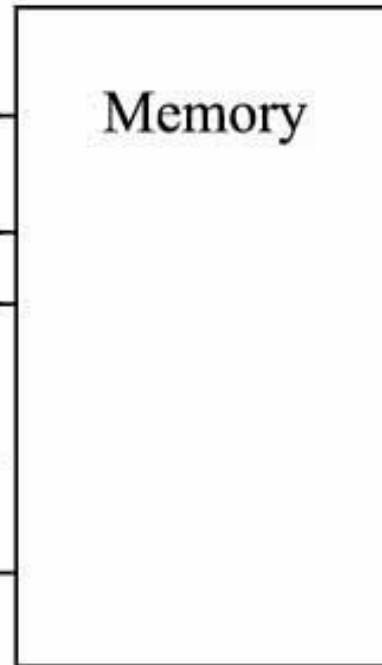
Little endian and each word at an address in multiples of 4

Step 1 Memory address which is multiple of 4

Chip Select

Read

Step 2 Memory using data bus returns the word (for instruction or data)



Address 0

LSB

1

LSB + 1

2

MSB - 1

3

MSB

$2^n - 4$

LSB

$2^n - 3$

LSB + 1

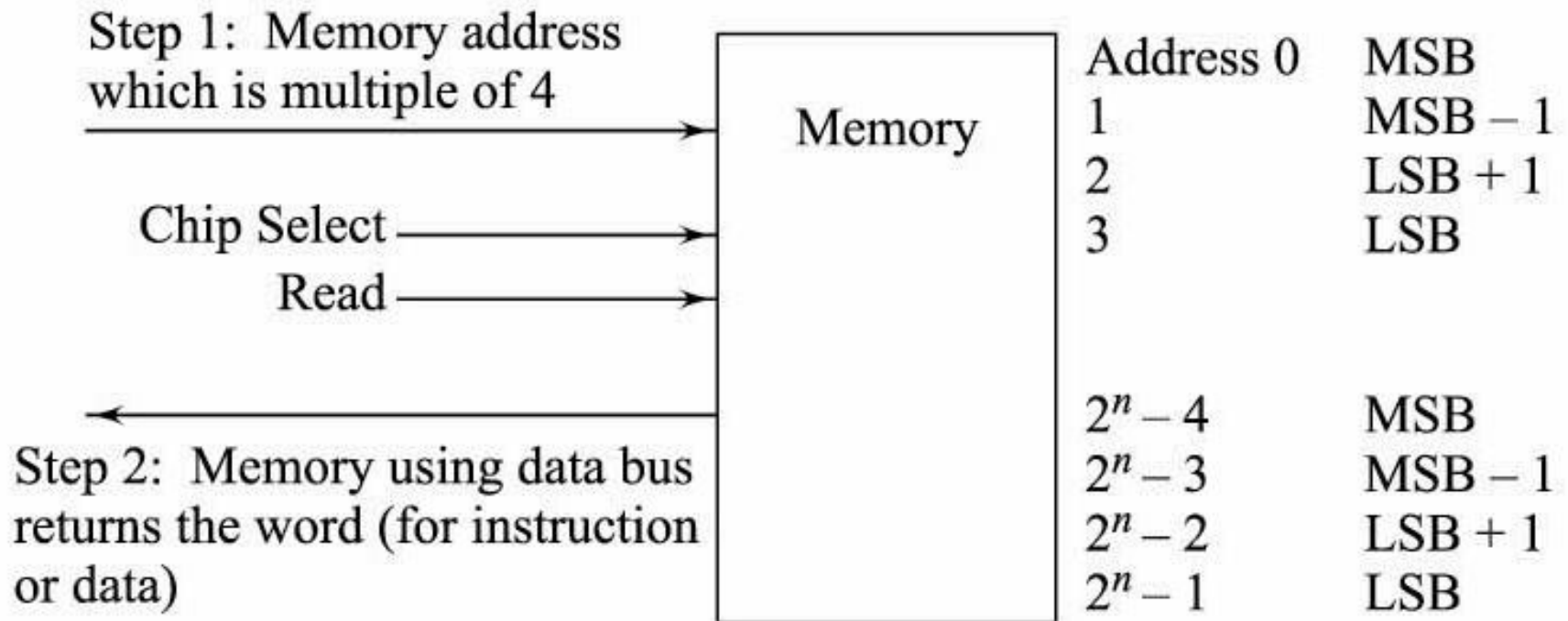
$2^n - 2$

MSB - 1

$2^n - 1$

MSB

Big endian and each word at an address in multiples of 4



Accessing a long word

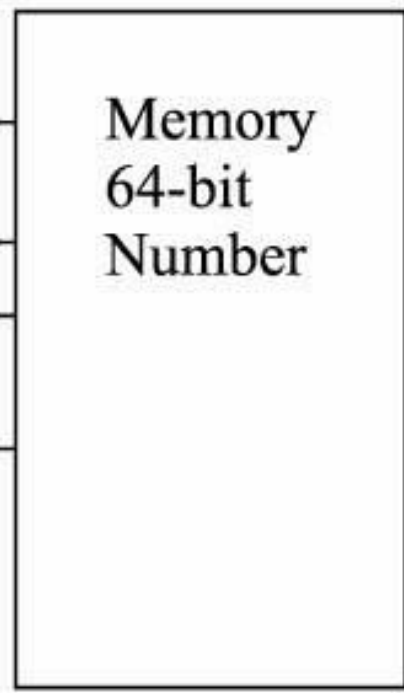
Accessing long word— Big endian and of 64-bits at address in multiple of 4

Step 1: Memory address, which is multiple of 4 as per data bus width of 32-bits



Chip Select

Read



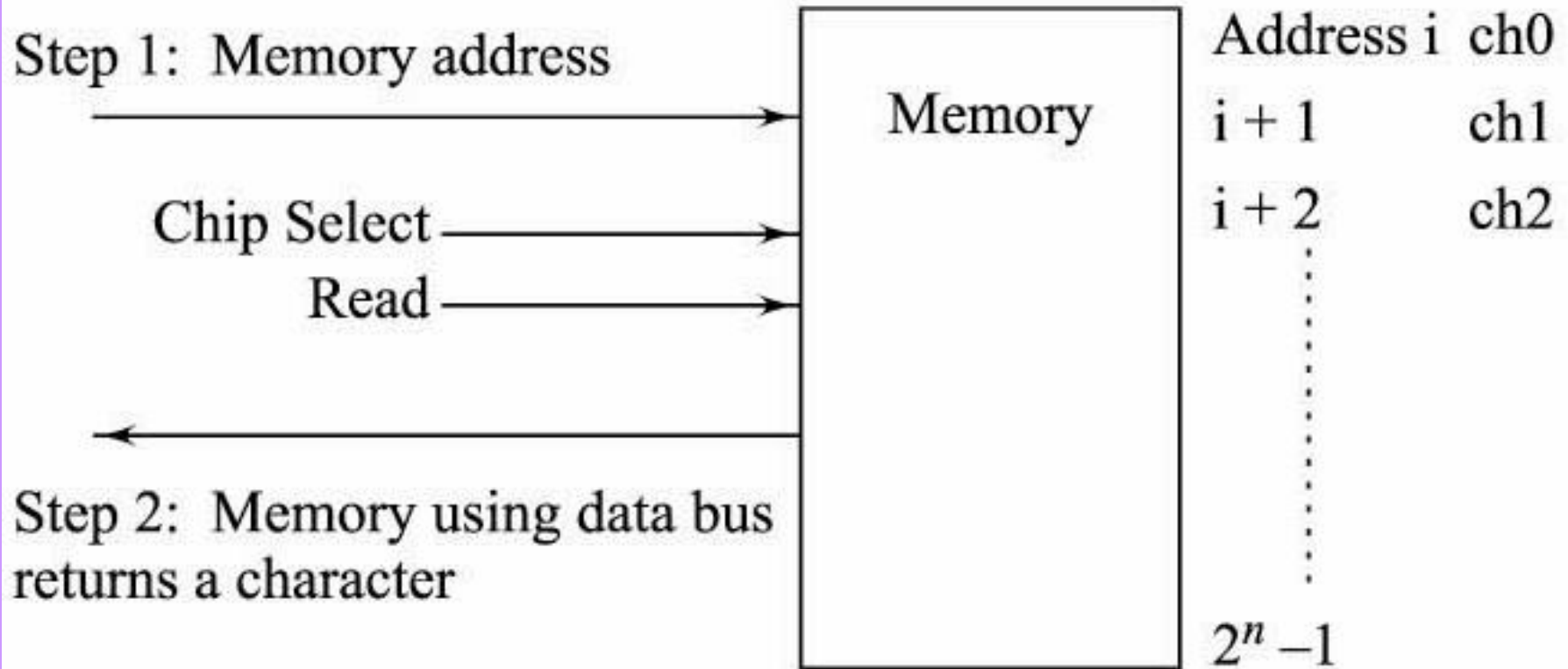
- Address 0... MSB
- 1..... MSB - 1
- 2..... MSB - 3
- 3..... MSB - 2
- 4..... LSB + 3
- 5..... LSB + 2
- 6..... LSB + 1
- 7..... LSb

Step 2: Memory using data bus returns the bytes for the word



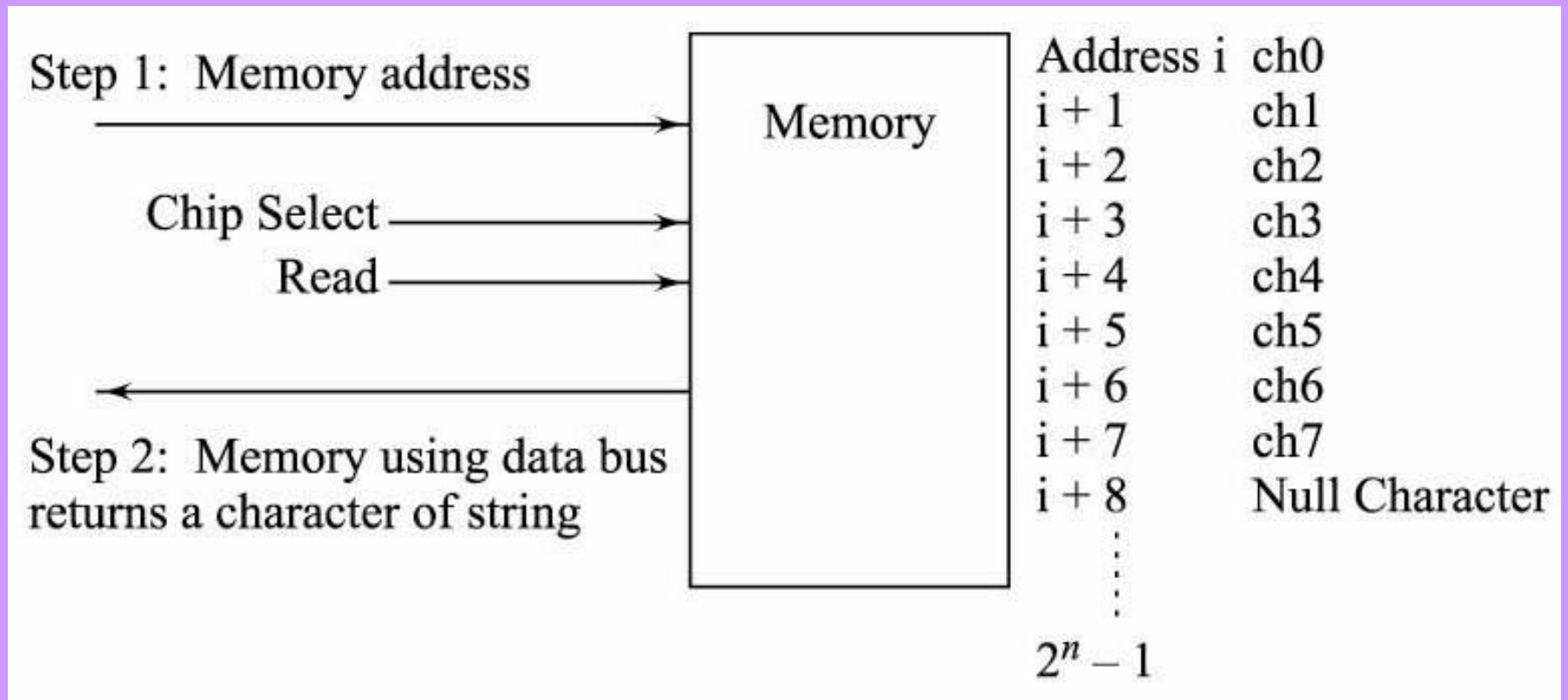
Accessing a character

Accessing a character (8-bit ASCII code) from a memory address



Accessing a string

Accessing a string (8-bit ASCII codes followed by null character) from memory addresses



Summary

We Learnt

- Alignment of bytes and words at memory and their fetch
- Fetching word, long word, characters and string

End of Lesson 06 on
Accessing the operands